FORMAL ENGINEERING REPORT
ON DEVELOPMENT
OF

MICROELEMENT TRANSISTORS

TASK 18

DECEMBER 10, 1962

MICRO-MODULE PROGRAM EXTENSION I

SIGNAL CORPS CONTRACT DA-36-039-SC-75066
SIGNAL CORPS SPECIFICATION SCL-6243
MARCH 17, 1958

RADIO CORPORATION OF AMERICA
SURFACE COMMUNICATIONS DIVISION
DEFENSE ELECTRONIC PRODUCTS
CAMDEN 2 NEW JERSEY

CONTENTS

GENERAL PURPOSE OF TASK

In order to demonstrate the feasibility of the Micro-Module Program two equipments using micro-modules have been designed and constructed. One is the AN/PRC-51 Helmet Radio and the other is the MicroPac Computer. The MicroPac represents the most densely packaged Tactical Field Computer in existence today.

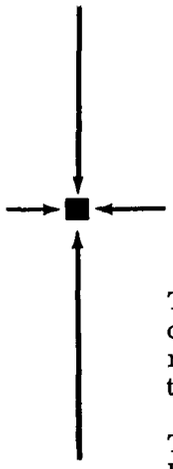
The Semiconductor Task 18 of Extension I of the Micro-Module Program was established to provide the transistors needed for the PRC-51 and the MicroPac. Every device developed in this task has found a use in one of the two equipments. Early in 1960 there were no reliable transistor packages, compatible with the basic requirements of the Micro-Module Program. A subtask was included in the semiconductor task to provide a transistor package for semiconductor vendors participating in this program. The major hardware achievement of this packaging subtask was the development of the .042 inch transistor header which has been standardized as the TO-46 transistor package. The TO-46 not only has become the most widely used transistor package in the Micro-Module Program but it also has been adopted by electronic equipment designers and producers wherever microminiature transistors are needed.

The Final Report on Transistors developed under the Micro-Module Program signifies the ending of effort required under Task 18. However, the Program, itself, constitutes a beginning of a scientific era which places a premium on high reliability and welcomes new packaging concepts. The successful accomplishment of the requirements of Task 18 has removed one of the major obstacles to industry wide acceptance of the Micro-Module Concept.

This semiconductor effort started in April of 1960. At that time transistor manufacturers were in the midst of an unnatural boom, where the supply could not meet the demand. Prices of semiconductors were astronomically high. Certain silicon switching and core driving transistors in TO-5 or TO-18 packages were selling for approximately $100 per unit.

A team of RCA and Signal Corps engineers visited major semiconductor manufacturers to determine industry attitudes toward the Micro-Module Program. Most companies had more business than they could handle. Semiconductor engineers were in short supply, and existing facilities were overtaxed with current production requirements.

The semiconductor industry was reluctant to take on new commitments to develop and repackage the transistors required for micromodules. Fortunately, there were some key personnel at various semiconductor plants who believed in the future potential of the micromodule. These persons convinced their managements to accept subcontracts from RCA for the various transistor subtasks. Today, the attitude of the semiconductor industry in regard to microelement semiconductors has changed from detached observance to active participation. Without exception, every major manufacturer in the semiconductor industry in the United States has produced microelement transistors and diodes. Almost all of the smaller semiconductor producers are also active participants in the Micro-Module Program. An illustration of the widespread industry acceptance of the Micro-Module Concept is the fact that many vendors at their own expense are now supplying devices and conducting test programs to qualify as second sources.



The success of the semiconductor task can be attributed to the vigorous activity and creative skill of the many persons located at the subcontractors' plants listed in this report. Assisted by the tireless efforts of the team of Signal Corps and RCA personnel, the various subcontractors were guided from a concept to successful accomplishment.

This Formal Engineering Report combines the achievements of the many persons in Industry and Government responsible for the present availability of microelement transistors. Their efforts and cooperation are hereby gratefully acknowledged by the Radio Corporation of America, the prime contractor for the Micro-Module Program.

ABSTRACT FOR PROGRAM

Task Eighteen of Micro-Module Program Extension I accomplished the repackaging in microelement form of six transistor devices. These are listed below with the companies subcontracted to perform the subtasks.

Task	Device	Company
18-1	2N706	Fairchild Semiconductor Corporation
18-2	2N699	Rheem Semiconductor Corporation
18-3	2N1132	Fairchild Semiconductor Corporation
18-5	2N697	Rheem Semiconductor Corporation
18-8	2N1094	Western Electric
18-9	2N404	Sylvania Electric Products

The successful completion of the above subtasks provided the Micro-Module Program with reliable transistors which are used in the AN/PRC-51 Helmet Radio Set and the MicroPac Computer.

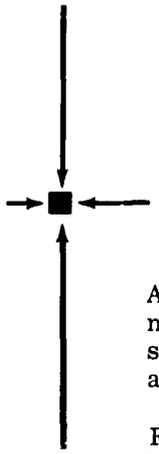
Millions of component hours of life test data have been accumulated at the plants of Radio Corporation of America and various subcontractors. This comprehensive testing program clearly established that the microelement transistors comply with the high reliability requirements of the Micro-Module Program.

Two accessory subtasks were included in the transistor effort. One was subtask 18-6 which resulted in the development of a transistor package compatible with the micromodule. At the start of this program there were no reliable miniature transistor packages suitable for use in micromodules. In order to provide backup support for the transistor subcontractors, a packaging program was undertaken. The major accomplishment of the packaging subtask was the development of the TO-46 transistor header.

The second additional subtask 18-7 established the source and tooling for ceramic wafers needed for the different transistors produced under Task 18. These wafers utilized molymanganese and nickel metalization and were suitable for mounting all of the transistor packages used in Extension I of the Micro-Module Program.

The successful completion of the packaging, wafer and transistor subtasks resulted in reliable microelement transistors.

Tasks 18-2 and 18-5 comprising the development of the 2N699 and 2N697 microelement transistors were performed by Rheem Semiconductor. In addition Fairchild Semiconductors has also qualified as a second source for these same devices. The latter company fabricated the stipulated number of samples and performed the required extensive testing at its own expense as a demonstration of Fairchild's faith in the future of the Micro-Module Concept and its applications.



All transistor manufacturers who participated in Task 18 successfully met the requirements of the purchase orders and applicable specifications. These subcontractors subsequently received approval of their microelement transistors produced under their assigned subtasks.

Final reports on the subtasks have been submitted by the various subcontractors. These individual reports have been consolidated into this one, all inclusive Formal Engineering Report on Microelement Transistors.

This combined report includes the individual final reports in separate numbered sections, as follows:

Section I (Task 18-1)	- The 2N706 transistor, Fairchild Semiconductor Corporation
Section II (Task 18-2)	- The 2N699 transistor, Rheem Semiconductor Corporation
Section III (Task 18-3)	- The 2N1132 transistor, Fairchild Semiconductor Corporation
Section IV (Task 18-4)	- VHF High Power transistor - not included herein since the task was reallocated as PEM Task 31-4 of Program Extension II
Section V (Task 18-5)	- The 2N697 transistor, Rheem Semiconductor Corporation
Section VI (Task 18-6)	- The Transistor Package
Section VII (Task 18-7)	- Ceramic Wafer for Transistor Microelement
Section VIII (Task 18-8)	- The 2N1094 Transistor, Western Electric Company
Section IX (Task 18-9)	- PNP Germanium Alloy 2N404 Transistor, Sylvania Electric Products, Inc.

CONCLUSIONS AND RECOMMENDATIONS

Individual conclusions and recommendations are indicated in the final reports for each subtask. Over-all conclusions encompassing the entire Task 18 are listed below.

1. All semiconductor vendors participating in the Transistor Task 18 successfully accomplished the repackaging of conventional devices into a configuration compatible with the Micro-Module Program.

2. The major packaging achievement of Task 18 was the TO-46 which has become an industry standard.

3. Microelement wafers suitable for mounting all reliable transistor package designs were developed under Task 18.

4. Transistors under Task 18, mounted on ceramic wafers also developed under this task, provided microelement transistors suitable for encapsulation into micromodules. These micromodules were used in the assembly of AN/PRC-51 Helmet Radios and the MicroPac Computer.

LIST OF PERSONNEL FOR TASK 18 PROGRAM OF EXTENSION I

The following personnel of the RCA Surface Communications Division contributed to the technical effort required on this Transistor Task.

Benjamin A. Andrews	Engineering Group Leader
Stephen S. Heller	Engineering Group Leader
George T. Hughes	Engineer
Paul K. Taylor	Engineering Editor
Frederick M. Weigert	Technician

SECTION I

FORMAL ENGINEERING REPORT

ON

MICROELEMENT 2N914 TRANSISTOR TYPE B-3
(Superseding 2N706)

TASK 18-1

MICRO-MODULE PROGRAM EXTENSION I

PO GX1-946254-7159-24-D38

FAIRCHILD SEMICONDUCTOR CORPORATION
545 WHISMAN ROAD
MOUNTAIN VIEW, CALIFORNIA

November 1962

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. PURPOSE OF TASK 18-1

On August 10, 1960 Fairchild Semiconductor received a contract from the Defense Electronics Division of the Radio Corporation of America at Camden, New Jersey, to develop a new and smaller semiconductor package suitable for mounting on Micro-Module wafers, the Fairchild 2N706 Silicon Mesa Transistor. The repackaging of this device was in no way to degrade from the high reliability of the device as encapsulated in the JEDEC (TO-18) package.

2. ABSTRACT

A new semiconductor package has been developed based on the outline dimensions of the JEDEC TO-18 with the following exceptions; the package height was decreased from 0.205 inches maximum to 0.065 inches maximum, and the diameter of the leads was decreased from 0.017 inches to 0.012 inches nominal wire size. The package was fabricated using standard Kovar hard glass sealing techniques. To insure hermeticity and decrease thermal resistance, the header was made from a solid Kovar slug. A thermal resistance of 87.5°C per watt has been established for this package containing a 2N914 transistor; measured from junction to heat sink. The TO-18 pin circle of 0.100 inches diameter and flange diameter of 0.210 inches were unchanged in the new package; this factor made possible the assembly of the package with existing assembly equipment. The engineering effort could therefore be concentrated on the package because of the elimination of the need for expensive large scale modifications to equipment and tooling necessary to accommodate the package. The development of the package by Fairchild was completed in March 1961. On April 18, 1962 the new package was standardized as the JEDEC TO-46.

In January 1961, Fairchild developed the 2N708 transistor; a planar version of the 2N706. This new device has a higher reliability than the 2N706 because of its passivated surface, it also has the advantage of a much lower leakage current. The 2N708 however had the disadvantage of lower speed switching characteristics than the 2N706. As a temporary means of supplying transistors to RCA, 2N708 devices were sorted to obtain the small percentage that could meet the switching speed requirements. This problem was overcome during March 1961 when Fairchild announced the 2N914, a Planar Epitaxial version of the 2N708. This new device has several advantages over its predecessors. Not only can the 2N914 meet the high speed switching requirements, but it also has the advantages of a much lower collector saturation voltage and lower leakage currents, as well as the stability advantages of a passivated surface. Figure 1-1 A, B, C, displays the basic construction techniques and advances in the state-of-the-art which made possible the evolution from the 2N706 Mesa, through the 2N708 Planar to the 2N914 Planar Epitaxial transistor.

Evaluation tests were conducted on the 2N914 device encased in the JEDEC TO-46 package. The transistors were subjected to storage life tests consisting of 1,000 hours at 200°C and to environmental life tests consisting of temperature cycling, moisture resistance, constant acceleration, vibration fatigue and shock. All tests were conducted in accordance with MIL-S-19500B, the RCA Specifications, and the

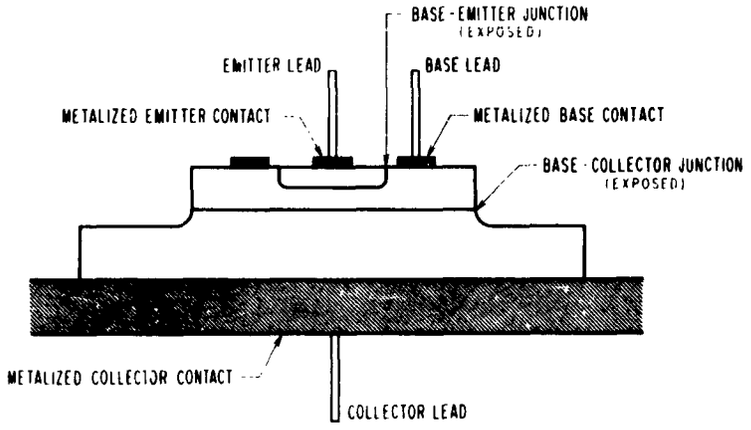


Figure 1-1A. 2N706 Double-Diffused Mesa Transistor

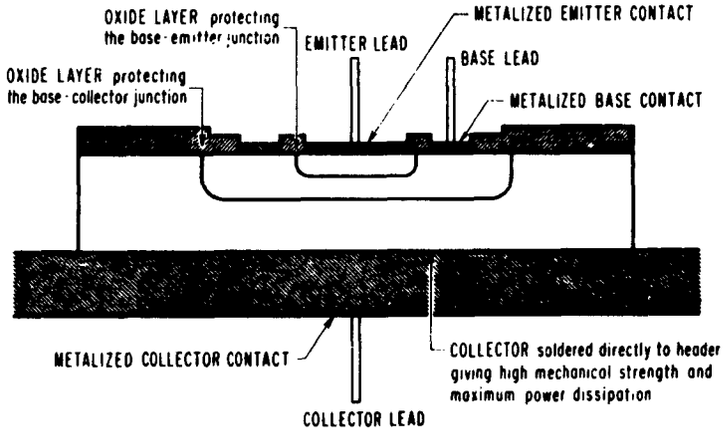


Figure 1-1B. 2N708 Double-Diffused Planar Transistor

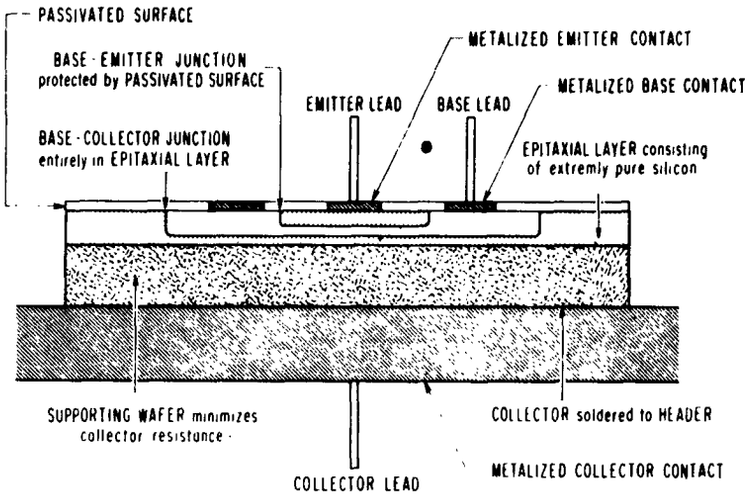


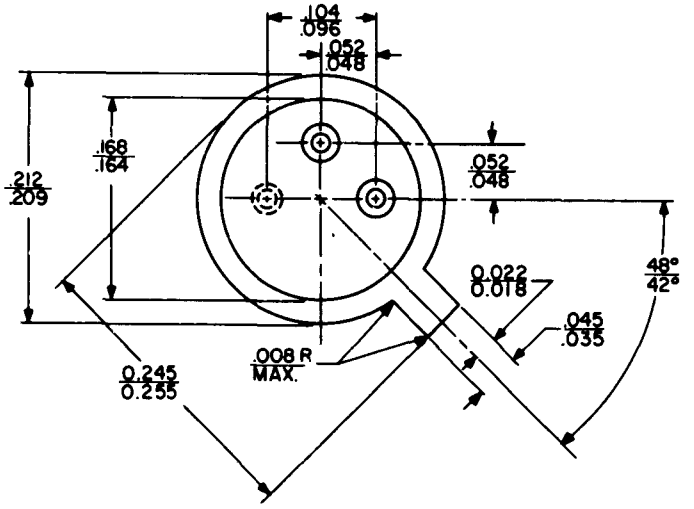
Figure 1-1C. 2N914 Double-Diffused Planar Epitaxial

Purchase Order. The reliability of the 2N914 encapsulated in the JEDEC TO-46 has been well established; as there were no failures during any of the tests performed on these transistors.

3. NARRATIVE AND DATA

3.1 DESIGN CONSIDERATIONS

It was specified that the package should be constructed using normal glass-to-metal sealing procedures, and that closure be made using resistance welding techniques. The package retained the flange and pin circle diameters and flange thickness of the JEDEC TO-18. The header was fabricated from a coined Kovar slug. The Kovar lead diameter was decreased from 0.017 inches to 0.012 inches nominal wire size. The thickness of the header was originally established at 0.035 inches; but was later increased to 0.045 inches to insure a hermetic seal. The headers were purchased from Veritron West Inc., of North Hollywood, California, an outside manufacturer of glass-to-metal seals. The can was stamped from electronic Grade A nickel. This material was selected because of its properties of weldability and corrosion resistance. Figures 1-2 and 1-3 are drawings of the header and can.



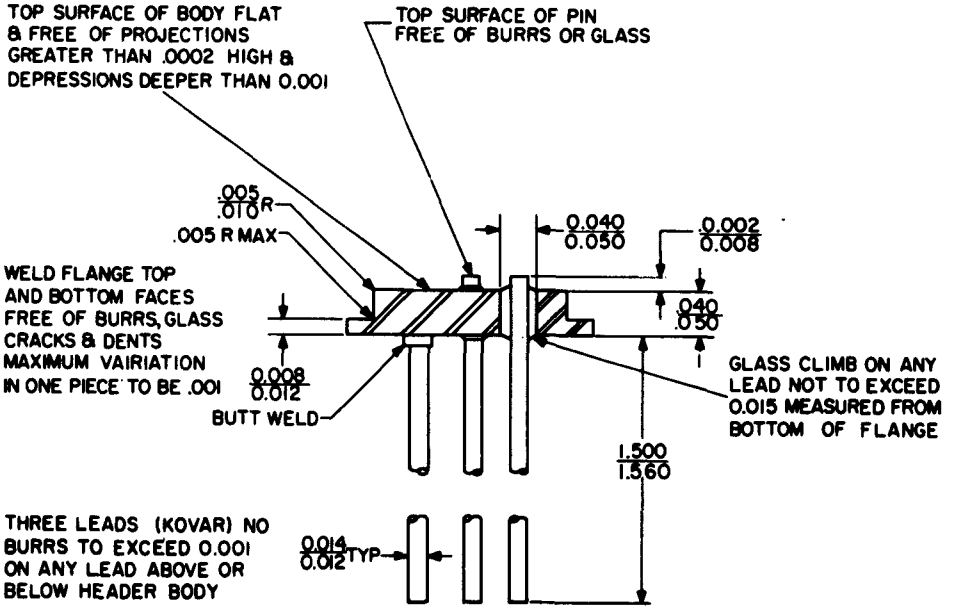


Figure 1-2. Transistor Header Assembly (TO-46)

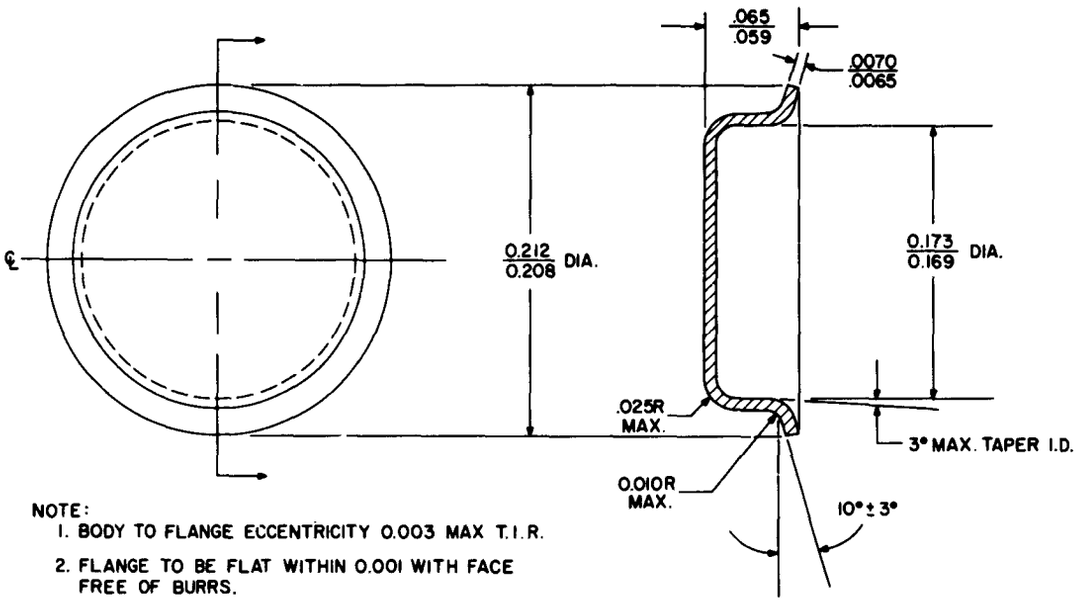


Figure 1-3. Transistor Can (TO-46)

3.2 FABRICATION PROCEDURES AND EQUIPMENT

3.2.1 DESCRIPTION OF PROCESS

The procedures used to assemble and encapsulate the 2N914 transistor in the TO-46 package do not differ from the methods used to encapsulate the same device in the JEDEC TO-18 package. The Process Flow Chart, Figure 1-4, displays the sequence of operation.

Materials and supplies used for assembly of the packages were inspected by the Quality Assurance Department prior to their release to the assembly line. Lot numbers and vendor identification were maintained on all material released to the assembly lines.

Electrically and visually sorted 2N914 dice were inventoried prior to assembly; lot identification was maintained through all assembly operations to insure adequate feed back of information to the processing and diffusion sections.

The first assembly operation was the bonding of the die to the header using a gold antimony eutectic as the bonding agent. The assembly was heated to 385°C to perform this operation. The gold emitter and base leads were then bonded to the aluminum patterns of the die. The assembly was heated to 370°C and the leads were thermal compression

PROCESS FLOW CHART

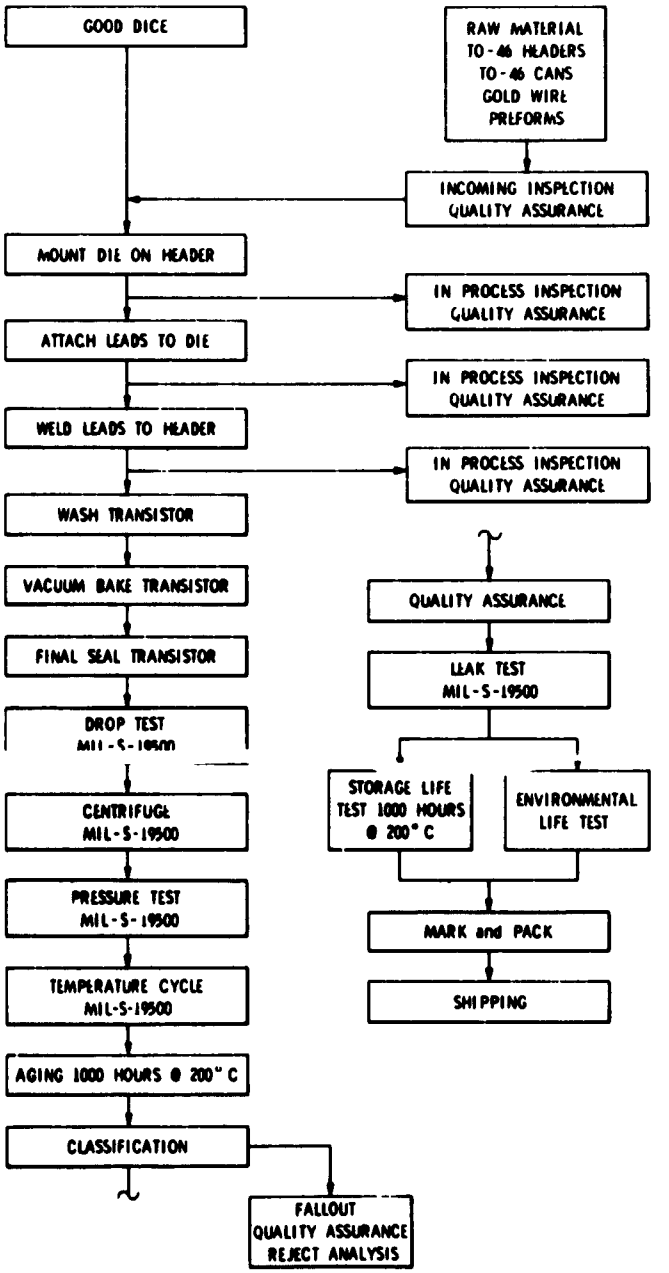


Figure 1-4. Transistor Fabrication Process Flow Chart

bonded to the aluminum using a tungsten carbide wedge. The emitter and base leads were then welded to the header pins using capacitor discharge dc welding techniques.

Random samples were inspected from each of the previous assembly operations by the Quality Assurance Department, and individual operator performance records were maintained. The individual performance records were posted to enable each operator to observe her own performance.

The transistor subassemblies were then washed with heated, deionized, distilled water and baked dry to remove any contaminants. The subassemblies were vacuum baked at 300°C under a pressure of 5×10^{-6} mm Hg for three hours. The transistors were encapsulated and welded in an inert controlled atmosphere. The moisture content of the nitrogen atmosphere in the dry box was continually monitored and at no time was allowed to exceed 120 ppm. Sample units were visually inspected and helium leak tested to insure proper welding.

All welded transistors were then subjected to environmental tests consisting of Drop, Temperature Cycle, Centrifuge and pressure tests. These tests were performed in accordance with MIL-S-19500B. The transistors were aged for 1,000 hours at 200°C to increase stability.

The transistors were electrically tested to the RCA specifications. The test equipment was programmed by the Electronic Maintenance Section. All electrical equipment were rechecked every four hours to insure proper programming. All electronic equipment and meters were calibrated against standards maintained by the Calibration Section.

Maintenance and calibration logs were maintained on all electronic equipment. All reject transistors were sent to Quality Assurance for Reject Analysis.

Random samples from each lot of tested transistors were taken by the Quality Assurance Department. These samples were retested to insure compliance with the specifications. These samples were not tested on production test equipment.

The tested transistors leak tested in accordance with MIL-S-19500B to insure hermeticity.

The transistors were then subjected to the Storage Life Tests and Environmental Life Tests as specified by RCA. All tests were conducted in accordance with MIL-S-19500, the RCA Specifications, and the Purchase Order.

After testing, the transistors were marked, packed, and processed for shipment.

3.2.2 EQUIPMENT

The TO-46 assembly equipment varied only slightly from the standard TO-18 assembly equipment. A standard TO-18 assembly jig was used in the Die Attach operation. The only modifications were a new heater nest to accommodate the header, and an improved direct reading controller to continuously monitor the heater temperature. A photograph of the Die Attach Jig is shown in Figure 1-5.

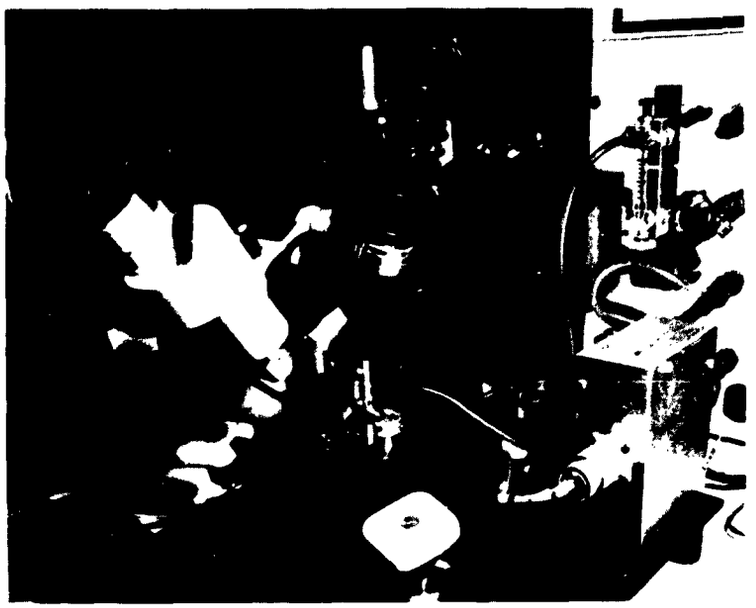


Figure 1-5. Die Attach Jig

The lead bond operations were performed using a standard TO-18 wedge lead bond jig. The heater nest was modified to accommodate the header and the same modifications were made to the heater controller that were incorporated in the Die Attach Heater Controller. A photograph of the Lead Bond Jig is shown in Figure 1-6.

Since the posts are very short, thermal compression bonding of the emitter and base leads to the posts was attempted. However, extensive centrifuge testing proved it to be unreliable and therefore this method was dropped. New upper and lower lead weld electrodes were then designed which would enable the lead wire to be welded to the posts. This system proved to be satisfactory. A photograph of the Lead Weld Jig is shown in Figure 1-7.

The assembly operations consisting of Wash, Vacuum Bake and Final Seal, as well as Environmental Testing Operations consisting of Drop, Centrifuge tests and Pressure Tests, Temperature Cycling and Aging did not require special equipment since all products manufactured by Fairchild are subjected to these tests. A photograph of the aging facilities is shown in Figure 1-8.

The electronic test equipment was designed and fabricated by the Instrumentation Division of Fairchild Semiconductor. A photograph of a Direct Readout h_{FE} Tester is shown in Figure 1-9.

Figure 1-6. Lead Bond Jig

Figure 1-7. Lead Weld Jig

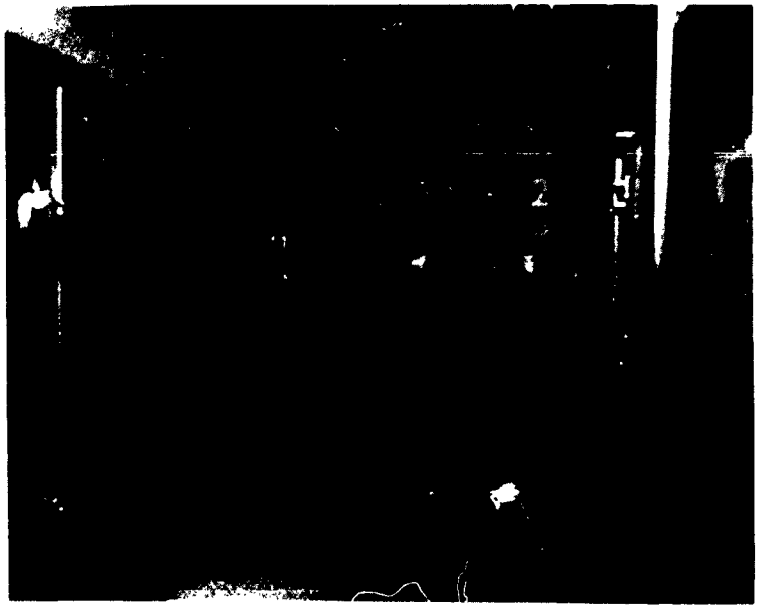


Figure 1-8. Aging Facilities

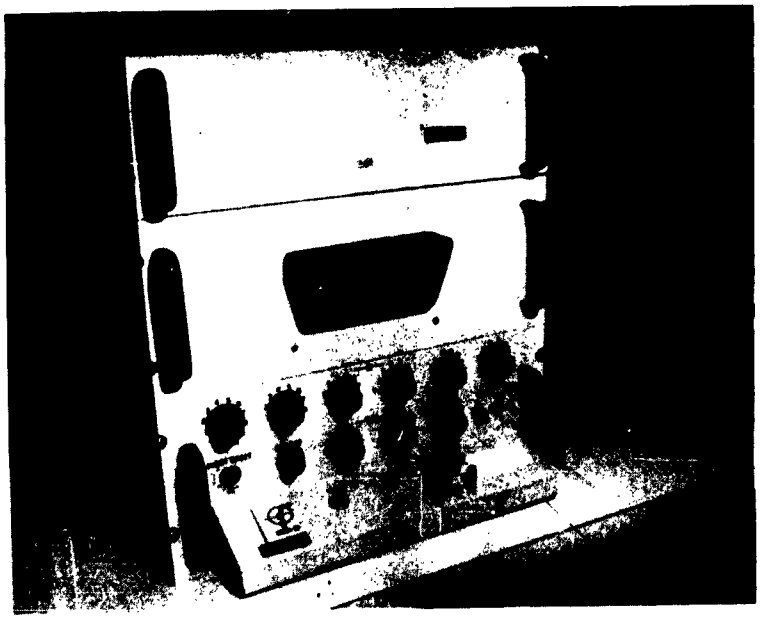


Figure 1-9. Direct Readout h_{FE} Tester

3.2.3 EVALUATION OF PROCESS AND EQUIPMENT

The assembly method does not vary from the standard TO-18 assembly processes and therefore large scale production of these transistors can be accomplished with a minimum of cost. Automation of the assembly processes of this transistor poses no greater problems than automation of the assembly processes of the 2N914 transistor encapsulated in the JEDEC TO-18 package.

3.3 TEST PERFORMANCE AND DATA

3.3.1 DESCRIPTION AND PURPOSE OF TESTS

After passing the electrical test requirements (Table 1-1) the transistors were subjected to Storage Life Tests and Environmental Tests. The transistors to be used in the Environmental Test were random samples taken from the lot. The remainder of the units were used in the Storage Life Tests. The Storage Life Tests consisted of aging for 1,000 hours at 200°C. The degradational and inoperable limits were defined and the failure rates for each condition were computed as Mean Time between Failures, and Fraction Defective per 1,000 hours. Distribution and stability of the parameters were plotted. The Environmental Tests consisted of three parts, Glass Seal Characteristics, Dynamic Characteristics, and Shock.

3.3.2 ANALYSIS OF PERFORMANCE DATA

A complete analysis of the tests performed and the data acquired for each parameter were compiled in two sections. The first section contains the analysis of the Storage Life Tests, the second section contains the analysis of the Environmental Tests. The test data summaries are contained in this report.

3.3.3 STORAGE LIFE TESTS

This section is an account of Storage Life testing at 200°C. This test was performed in accordance with paragraphs 40.7, 40.7.1 and 40.7.1.1 of MIL-S-19500B.

We have defined both degradational and inoperable limits and computed the failure rates for each condition as Mean Time Between Failures and Fraction Defective per 1000 hours.

To complete the presentation, both the distribution and stability of the test parameters are plotted. For parameter distribution, the 10th, 50th, and 90th percentiles of the samples are shown. For parameter stability the charts show the changes in the test parameters from their initial readings.

There were no failures on this test.

TABLE 1-1

GROUP A TEST REQUIREMENTS FOR MICROELEMENT 2N914 TRANSISTORS

(Pertinent Specification A-8948865, Revision B)

Test	Conditions	Sym.	Min.	Max.	Unit
Group A					
*Collector cut-off current	VCB = 15V IE = 0	ICBO	-	15	muAdc
*Collector-base breakdown voltage	IC = 100 ua IE = 0	BV_{CBO}	25	-	Vdc
*Collector emitter voltage	RBE = 10 ohms ICER = 50 ma (pulse) PW = 167 usec. duty cycle = 2%	LV_{CER}	20	-	Vdc
*Emitter cut-off current	VEB = 3V IC = 0	IEBO	-	10	uAdc
*Base emitter saturation voltage	IC = 18 ma IB = 1 ma	VBE(sat)	-	1.0	Vdc
*Small signal current gain	VC = 10V IC = 15 ma f = 100 mc	h_{fe}	2	-	
*DC forward current transfer ratio at TA = -30°C	VCE = 0.7V IC = 18 ma	h_{FE}	20	-	
*DC forward current transfer ratio at TA = -55°C	VCE = 0.7V IC = 18 ma	h_{FE}	15	-	
*Turn on time *Turn off time (see circuits 4.1.2)	IC = 20 ma IB_1 = 2 ma IB_2 = 1 ma	td + tr ts + tf	- -	50 60	Musec Musec
*Output Capacitance	VCB = 10V IE = 0	C_{OB}	-	6	uuf
*Collector cut-off current at 125°C	VCB = 15V IE = 0 TA = 125° ± 3°C	ICBO	-	15	uAdc
*Collector-emitter saturation voltage	IC = 18 ma IB = 1 ma TA = 125° ± 3°C	VCE(sat)	-	0.25	Vdc
*Thermal resistance (see 4.1.3)	T_j = 200°C	Q_j-c	-	250	°C/W

TABLE 1-2
ANALYSIS OF STORAGE LIFE (GROUP C) TESTS

TYPE TESTED
2N914 (B-3)
PARAMETER
MFG. PERIOD: April 1961
DATE ISSUED: September 1961

FAILURE RATE

ENVIRONMENT	DEGRADATIONAL		INOPERABLE	
	MTBF	FRACTION DEF.	MTBF	FRACTION DEF.
200°C Storage	$\geq$ 273,000 hrs (60% confidence	$\geq$ .0037 per 1,000 hrs	$\geq$ 273,000 hrs	$\geq$ .0037 per 1,000 hrs

FAILURE ANALYSIS

SAMPLE SIZE	TOTAL HOURS	FAILURES	250 HOUR FAILURES	500 HOUR FAILURES	1000 HOUR FAILURES
250	250,000	0 degradation			
	250,000	0 Inoperable			

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS	INITIAL LIMITS		END OF LIFE LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
ICBO	VCB = 15 Vdc TA = 25°C		1 μadc		1 μadc		1 μadc
IEBO	VEB = 3 Vdc TA = 25°C		20 μadc		20 μadc		20 μadc
HFE	Vce = 1 Vdc Ic = 18 mAdc TA = -30°C	18		18		18	
VCE (Sat)	IC = 18 mADC Ib = 1 mAdc TA = 125°C		1.2 Vdc		1.2 Vdc		1.2 Vdc

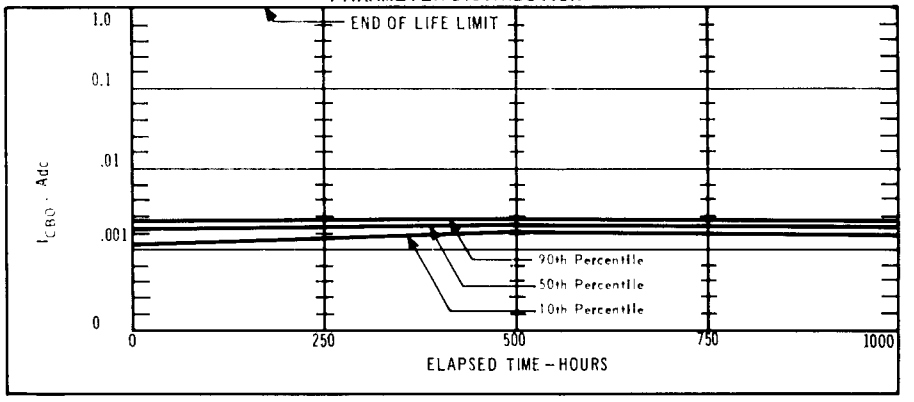
TABLE 1-3
I_{CBO} PARAMETER ANALYSIS

PARAMETER TEST CONDITIONS	
TEST CONDITIONS	PARAMETER MEASURED
V_{CB} = 15Vdc TA = 25°C	I_{CBO}
LIFE TEST CONDITIONS	
TEMPERATURE	ENVIRONMENTAL STRESS
200°C	Storage

PARAMETER TEST LIMITS and SUMMARY		
INITIAL LIMITS		SAMPLE SIZE
MIN.	MAX.	
	1 μAdc	250
END OF LIFE LIMIT		UNITS EXCEEDING END OF LIFE LIMIT
MIN.	MAX.	
	1 μAdc	0
INOPERABLE LIMIT		UNITS EXCEEDING INOPERABLE LIMIT
MIN.	MAX.	
	1 μAdc	0

TYPE 2N914	TESTED (B-3)
PARAMETER I_{CBO}	
MFG. PERIOD April 1961	
DATE ISSUED September 1961	

PARAMETER DISTRIBUTION



PARAMETER STABILITY

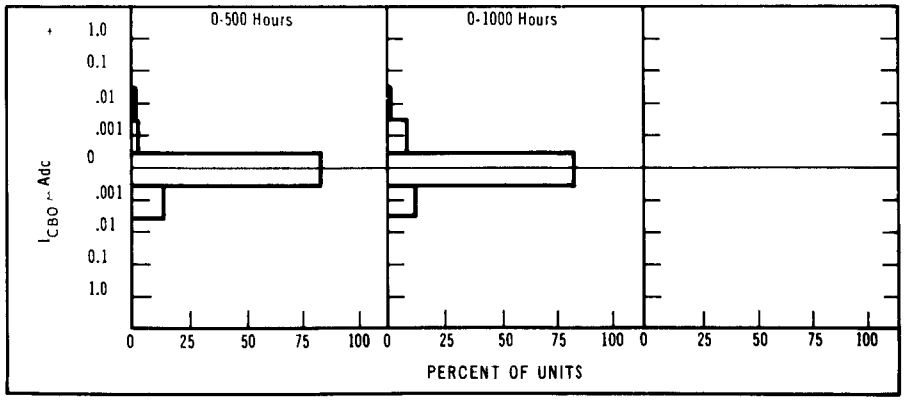


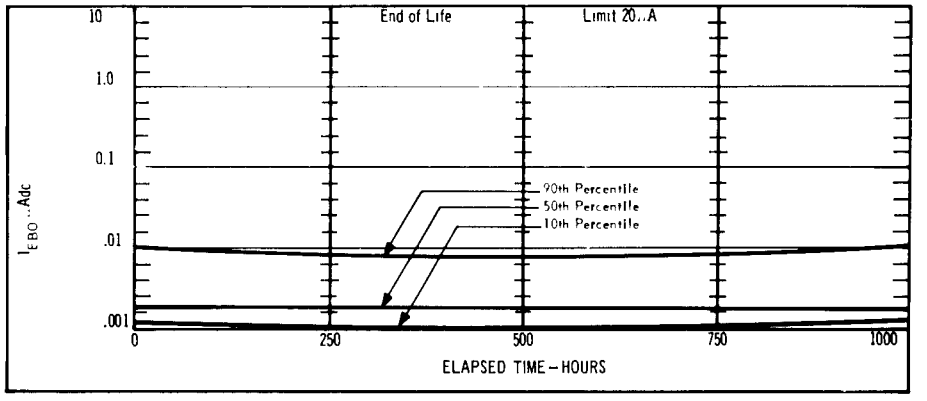
TABLE 1-4
I_{EBO} PARAMETER ANALYSIS

PARAMETER TEST CONDITIONS	
TEST CONDITIONS	PARAMETER MEASURED
V_{EB} = 3Vdc TA = 25°C	I_{EBO}
LIFE TEST CONDITIONS	
TEMPERATURE	ENVIRONMENTAL STRESS
200°C	Storage

PARAMETER TEST LIMITS and SUMMARY		
INITIAL LIMITS		SAMPLE SIZE
MIN.	MAX.	
	20 μAdc	250
END OF LIFE LIMIT		UNITS EXCEEDING END OF LIFE LIMIT
MIN.	MAX.	
	20 μAdc	0
INOPERABLE LIMIT		UNITS EXCEEDING INOPERABLE LIMIT
MIN.	MAX.	
	20 μAdc	0

TYPE 2N914	TESTED (B-3)
PARAMETER I_{EBO}	
MFG. PERIOD April 1961	
DATE ISSUED September 1961	

PARAMETER DISTRIBUTION



PARAMETER STABILITY

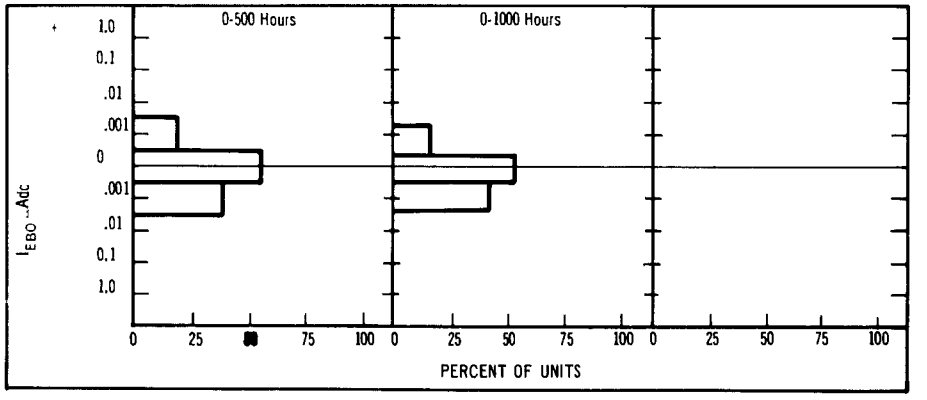


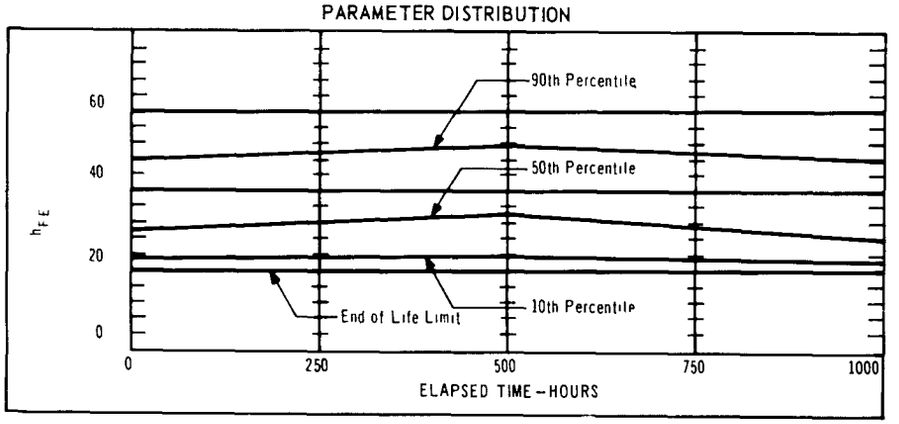
TABLE 1-5
h_{FE} PARAMETER ANALYSIS

PARAMETER TEST CONDITIONS	
TEST CONDITIONS	PARAMETER MEASURED
V_{CE} = 1Vdc I_C = 17mA	h_{FE}
LIFE TEST CONDITIONS	
TEMPERATURE	ENVIRONMENTAL STRESS
200°C	Storage

PARAMETER TEST LIMITS and SUMMARY		
INITIAL LIMITS		SAMPLE SIZE
MIN.	MAX.	
18		250
END OF LIFE LIMIT		UNITS EXCEEDING END OF LIFE LIMIT
MIN.	MAX.	
18		0
INOPERABLE LIMIT		UNITS EXCEEDING INOPERABLE LIMIT
MIN.	MAX.	
18		0

TYPE TESTED 2N914 (B3)
PARAMETER h_{FE}
MFG. PERIOD April 1961
DATE ISSUED September 1961

PARAMETER DISTRIBUTION



PARAMETER STABILITY

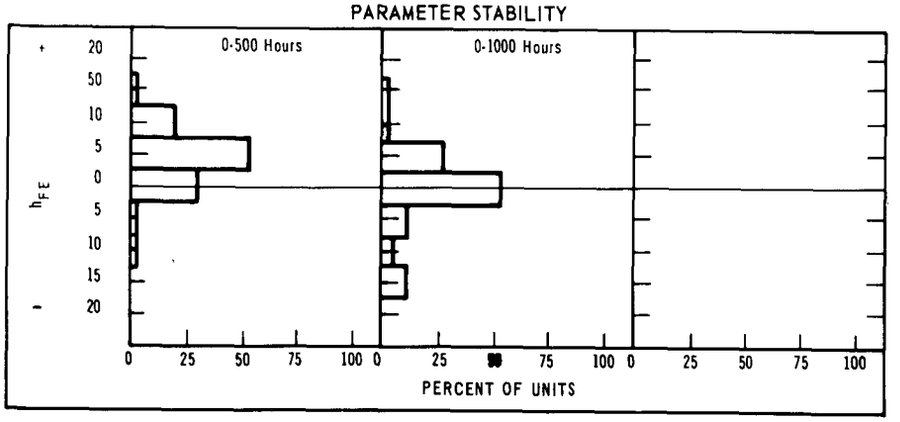


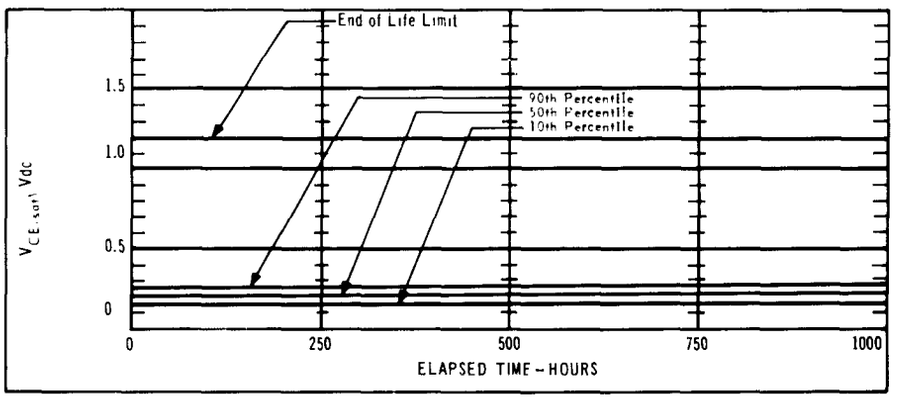
TABLE 1-6
V_{CE} PARAMETER ANALYSIS

PARAMETER TEST CONDITIONS	
TEST CONDITIONS	PARAMETER MEASURED
I_C = 18 mAdc I_B = 1 mAdc TA = 125°C	$V_{CE(sat)}$
LIFE TEST CONDITIONS	
TEMPERATURE	ENVIRONMENTAL STRESS
200°C	Storage

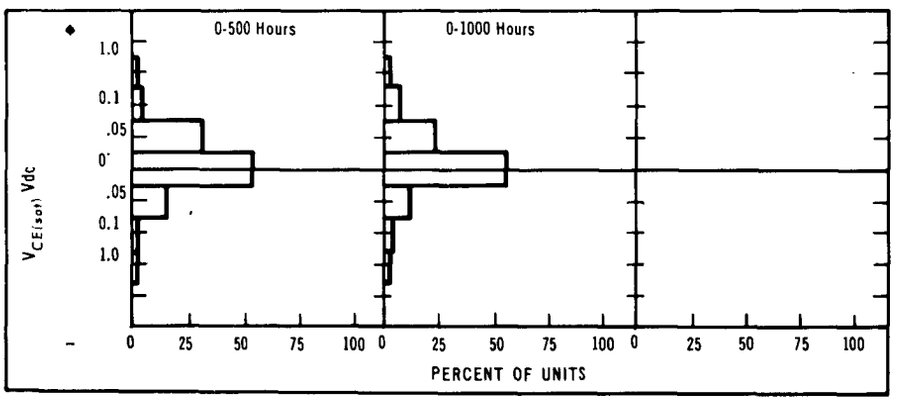
PARAMETER TEST LIMITS and SUMMARY		
INITIAL LIMITS		SAMPLE SIZE
MIN.	MAX.	
	1.2Vdc	250
END OF LIFE LIMIT		UNITS EXCEEDING END OF LIFE LIMIT
MIN.	MAX.	
	1.2Vdc	0
INOPERABLE LIMIT		UNITS EXCEEDING INOPERABLE LIMIT
MIN.	MAX.	
	1.2Vdc	0

TYPE TESTED	2N914 (B-3)
PARAMETER	$V_{CE(sat)}$
MFG. PERIOD	April 1961
DATE ISSUED	September 1961

PARAMETER DISTRIBUTION



PARAMETER STABILITY



3.3.4 ENVIRONMENTAL TEST

This Environmental Test section of the report reflects testing on devices produced during the period of April through September 1961. Test samples were selected at random from the lot. All Environmental Tests were performed in accordance with MIL-S-19500B. The same initial and post test limits were used here as were used for Life Tests.

This section of the report is divided into three subgroups which conform to the order of testing. During Subgroup I, testing for glass seal characteristics, all units were checked for moisture resistance, and were Temperature Cycled. During Subgroup II - testing for dynamic characteristics, - the units were subjected to constant (Centripetal) acceleration and fatigue. Testing is completed with Subgroup II, a shock test.

The data of these tests and an analysis of the results are contained in the following tables.

There were no failures as a result of these tests.

TABLE 1-7
ENVIRONMENTAL TEST ANALYSIS (TEMPERATURE AND MOISTURE)

TYPE	TESTED
2N914	B3
PARAMETER	
MFG. PERIOD	April 1961
DATE ISSUED	August 15, 1961

SUBGROUP I – GLASS SEAL

These tests conform to the requirements of MIL-STD 19500B Paragraph 40.14 and 40.6

ENVIRONMENTAL CONDITIONS

Temperature Cycling – 10 cycles; each cycle consisting of 15 minutes at 165°C, 5 minutes at 25°C, 15 minutes at 200°C and 5 minutes at 25°C

Moisture Resistance – ten (10) 24 hour cycles; each cycle consisting of variable temperature between –10°C and +65°C and variable relative humidity between 80% and 98%

FAILURE ANALYSIS

SAMPLE SIZE	FAILURES	CLASSIFICATION OF FAILURES
10	0 degradation 0 inoperable	

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS	INITIAL LIMITS		POST TEST LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	V_{CB} = 15V		1.0 μa		1.0 μa		1.0 μa
I_{EBO}	V_{EB} = 3V		20 μa		20 μa		20 μa
h_{FE}	I_C = 18 mA V_{CE} = .7V TA = -30°C	18		18		18	
$V_{CE(sat)}$	I_C = 25 mA I_B = 2 mA TA = 125°C		1.2V		1.2V		1.2V

TABLE 1-8
ENVIRONMENTAL TEST ANALYSIS (CENTRIFUGE AND VIBRATION)

TYPE	TESTED
2N914	B3
PARAMETER	
MFG. PERIOD	April 1961
DATE ISSUED	August 15, 1961

SUBGROUP II – DYNAMIC

These tests conform to the requirements of MIL-STD 19500B Paragraphs 40.18 and 40.20

ENVIRONMENTAL CONDITIONS

Constant Acceleration	– 1 minute at 20,000 g in each of three orientations (3 minutes total)
Vibration Fatigue	– 32 hours of harmonic motion with constant 20g peak acceleration at 40 to 100cps in each of three orientations (96 hours total)

FAILURE ANALYSIS

SAMPLE SIZE	FAILURES	CLASSIFICATION OF FAILURES
6	0 degradation 0 inoperable	

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS	INITIAL LIMITS		POST TEST LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	V_{CB} = 15V		1.0 μa		1.0 μa		1.0 μa
I_{EBO}	V_{EB} = 3V		2.0 μa		20 μa		20 μa
h_{FE}	I_C = 18mA V_{CE} = .7V TA = -30°C	18		18		18	
$V_{CE(sat)}$	I_C = 25mA I_B = 2mA TA = 125°C		1.2V		1.2V		1.2V

TABLE 1-9
ENVIRONMENTAL TEST ANALYSIS (SHOCK)

TYPE TESTED
2N914 B3
PARAMETER
MFG. PERIOD April 1961
DATE ISSUED August 15, 1961

SUBGROUP III – SHOCK

These tests conform to the requirements of MIL-STD 19500B Paragraph 40.10

ENVIRONMENTAL CONDITIONS

Shock – 5 Blows at 1500 g, 0.5 millisecond duration in each of four orientations.

FAILURE ANALYSIS

SAMPLE SIZE	FAILURES	CLASSIFICATION OF FAILURES
6	0 degradation 0 inoperable	

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS	INITIAL LIMITS		POST TEST LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	V_{CB} = 15V		1.0 μa		1.0 μa		1.0 μa
I_{EBO}	V_{EB} = 3V		20 μa		20 μa		20 μa
h_{FE}	I_C = 18 mA V_{CE} = .7V TA = −30°C	18		18		18	
$V_{CE(sat)}$	I_C = 25 mA I_B = 2 mA TA = 125°C		1.2V		1.2V		1.2V

3.4 UNIT SPECIFICATIONS

The transistors were physically and electrically tested in accordance with the following specifications:

RCA dwg. A-8978123 Hermetic Package for Micro-Transistors

RCA dwg. A-8972091 General Specifications for Micro-Transistors

RCA dwg. A-8948865 Type B-3 Transistors

The information contained in 3.3.3 and 3.3.4, above, indicate Fairchild's conformance to all the specified requirements. The electrical specifications were much more stringent than the EIA specifications for a 2N706. In fact, only a very small percentage of 2N706 transistors could meet the specifications. For this reason the tests were conducted using 2N914 transistors.

3.5 PRODUCT EVALUATION

In large production quantities, assembly and encapsulation of the 2N914 transistor in the JEDEC TO-46 package can be accomplished at a cost approximating the assembly costs of the same transistors in the JEDEC TO-18 package. The technical advances in assembly tooling and automation will be applicable to the assembly of both packages. These factors will contribute to a much lower manufacturing cost, and will eliminate duplication of equipment. A photograph of the 2N914 microelement transistor is shown in Figure 1-10 adjacent to a desk key for size comparison.

3.6 DELIVERY

The delivery schedule of transistors shipped to RCA is as shown below:

Quantity Required	Date Required	Quantity Shipped	Date Shipped	Transistor Type	Use of Transistors
50	12-1-60	50	12-14-60	2N706 Mesa	Signal Corps Tests
100	1-1-61	100	1-18-61	2N706 Mesa	Hermiticity Tests
50	2-1-61	50	2-6-61	2N706 Mesa	Signal Corps Tests
150	2-1-61	22	2-6-61	2N706 Mesa	"B" Tests
		128	4-24-61	2N706 Mesa	2000 Hr. Tests
100	4-1-61	100	10-17-61	2N708 Planar	2000 Hr. Tests
200	7-1-61	200	10-10-61	2N914 Planar Epitaxial	2000 Hr. Tests
100	8-1-61	50	10-10-61	2N914 Planar Epitaxial	Signal Corps Tests
		50	10-17-61	2N914 Planar Epitaxial	Signal Corps Tests

Figure 1-10. (Task 18-1) Fairchild Semiconductor 2N914 Microelement Transistor (Magnification 5x)

4. CONCLUSIONS AND RECOMMENDATIONS

4.1 CONCLUSIONS

It was concluded that a minimum seal length of 0.040 inches is necessary to insure a hermetic seal ot the leads with present glass-to-metal seal technology. It was concluded that thermal compression bonding of the lead wires to the posts is not favorable and that a resistance weld must be used to insure high reliability. It was concluded from the tests conducted that the Fairchild 2N914 transistor encased in the JEDEC TO-46 package is a reliable device.

4.2 RECOMMENDATIONS

The tests were conducted on a relatively small number of transistors, and even though there were no failures as a result of any of the tests conducted; it is recommended that similar tests be conducted on a sufficiently large number of transistors, to more adequately support these findings.

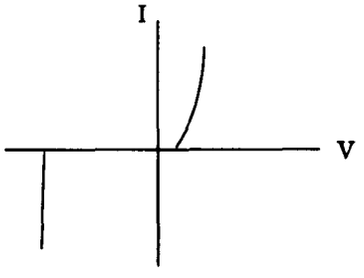
APPENDIX A. TRANSISTOR FAILURE ANALYSIS

FAIRCHILD SEMICONDUCTOR CORPORATION

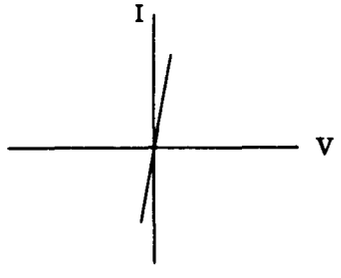
October 4, 1961

Subject: RCA B-3 TRANSISTOR (2N914) UNIT #146

The 2N914 transistor which failed at RCA after 2000 hours storage at 200°C was analyzed by several members of the Quality Control and Reliability Department. Curve tracer analysis showed that collector-base, emitter-base, and collector-emitter were dead shorts. The unit was uncapped and examined at a magnification of 250X. A path from emitter bond to base bond was observed, which usually suggests application of excessive current or power during testing. The internal leads were carefully lifted with a probe to assure that they were not bridging the junctions and the transistor was retested. The results did not change. The trace of the collector-base junction of a good NPN transistor is drawn below as well as the trace of the collector-base junction of the rejected transistor.



Good CB Characteristic



RCA B-3 #146

Even a transistor whose collector-base has degraded and softened will not avalanche when forward biased until it reaches approximately .7 volt. The fact that this transistor exhibits a collector-base breakdown which is completely linear or resistive in both directions, as well as the fact that it shows the characteristic path from emitter to base, pretty well confirms that it was damaged during testing. A photomicrograph of the transistor die is shown in Figure 1-11.

Figure 1-11. Photomicrograph of Transistor Die

SECTION II

FORMAL ENGINEERING REPORT
ON
MICROELEMENT 2N699 TRANSISTOR, TYPE: HIGH VOLTAGE SWITCHING
TASK 18-2
MICRO-MODULE PROGRAM EXTENSION I

PO GX1-946253-5773-24-D38

RHEEM SEMI-CONDUCTOR OPERATION OF RAYTHEON COMPANY
MOUNTAIN VIEW, CALIFORNIA

August 15, 1962

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. PURPOSE OF TASK 18-2

The purpose of this contract was to design and supply test units and test data for 2N699 transistors in packages suitable for mounting on Micro-Module wafers and with electrical, environmental, and mechanical properties as described in Task 18-2, the Rheem proposal to RCA dated May 17, 1960, subsequent correspondence, and purchase orders.

2. ABSTRACT

A microelement transistor package has been developed and the required 2N699 transistors have been encapsulated and tested in this package to RCA specifications referred to in Task 18-2. The development has resulted in a highly reliable unit.

At the inception of this project (Micro-Module Task 18-2) a similar project (Task 18-5 on 2N697 microelement transistors) had been underway for approximately eight months. Since the package requirement for the present project was very similar, full advantage was taken of the design and development already completed. For a description of the package development on the earlier project, reference should be made to Section V of this combined report.

It is believed that the .065" package height, the result of this project, is a minimum for the present state-of-the-art of header fabrication and semiconductor processing. The work done on internal lead configuration and bonding techniques in order to minimize height also has resulted in a unit which is substantially more resistant to shock. Another feature that will increase the reliability of any device encapsulated in this package is its relatively low thermal resistance. The final design has a thermal resistance of less than 50°C/watt as compared to 68°C/watt for a conventional Kovar TO-5, measured from junction to heat sink, and containing 2N699 type transistors.

3. NARRATIVE AND DATA

3.1 DESIGN CONSIDERATIONS

The development, herein described, of the microelement 2N699 transistor Task 18-2, started eight months after the initiation of a similar project for the microelement 2N697 transistor (Task 18-5). The package requirement for the two devices was very similar and, consequently, advantage was taken of the package development work done for the earlier unit. For an account of this earlier package development reference should be made to Section V of this report.

When this project began the package development had already settled on the type of package shown in Figures 5-1 and 5-2, Section V. At this time a great number of headers of 35 mil thickness had been tested. However, after some discussion with RCA and the Signal Corps it was decided to change to the 45 mil header thickness (therefore, also a 45 mil, glass-metal seal length). This is discussed in more detail in section 3.3.4 of this report section.

Another major design change, that became necessary during the course of this development, pertained to the internal lead configuration and lead bonding method. This problem, which arose after delivery of the initial 300 units, is discussed in section 3.3.4.

3.2 FABRICATION PROCEDURES AND EQUIPMENT

3.2.1 and 3.2.2 DESCRIPTION OF PROCESS AND EQUIPMENT

The design and experimental work on the package was done jointly with two outside vendors of glass-to-metal seals. These were ITT Farnsworth of Palo Alto, California, and Zell Products of Norwalk, Connecticut. The devices for this task were supplied from Rheem's existing production of 2N699 dice. The earlier development of transistor microelement 2N697 had brought about the modification of an existing TO-18 production line to handle its lower height headers. Most of the changes in fabrication procedure and equipment for project had to do with the change in lead bonding procedures, discussed later in this report. Other minor changes from the Rheem TO-18 process involved slight modifications of parts handling procedures and weld cycles at final sealing. Rheem fabrication equipment was used throughout the line with the exception of the lead bonder and the welder portion of the final seal and bake-out unit. Figure 5-5 of Section V shows the Kullicke and Soffa Model 401 lead bonder that was used. Figure 5-6 of the same section shows a photograph of the final seal and bake-out unit.

3.2.3 EVALUATION OF PROCESS AND EQUIPMENT

The process and equipment involved in development of the 2N699 transistor were identical to those used for the 2N697 described on page 6 of Section V.

3.3 TEST PERFORMANCE AND DATA

3.3.1 DESCRIPTION AND PURPOSE OF TESTS

The testing program for the Rheem 2N699 microelement transistors includes tests by the vendor and tests by RCA. These were made to assure adherence to the requirements of RCA Specification A-8948874. All transistors shipped to RCA on this program (Task 18-2) were aged at 200°C for 1000 hours and then each unit was required to pass the stipulated electrical performance (Group A) tests before subjection to Group C and/or Group B tests.

The second 1000 hours of the Storage Life Test (Group C) at 200°C was performed at RCA, Camden, N.J. on all of the 200 units received from the vendor. Group B environmental tests were also performed at RCA in three groups of ten units each. Group I was subjected to Thermal Shock and Moisture Resistance, Group II was given Centrifuge and Vibration tests, and Group III was subjected to the Shock Test.

3.3.2 and 3.3.3 ANALYSIS OF PERFORMANCE DATA AND TEST PROCEDURES

Table 2-1 lists the electrical performance requirements (Group A tests) which must be met by all 2N699 transistors before undergoing Group B and/or Group C tests, and Tables 2-2 and 2-3 exhibit the type of test, the procedures and the data taken, respectively, for the Group B (Environmental) test and the Group C (Storage Lift) test. Figures 2-1, 2-2, and 2-3 are graphs showing the respective distributions of I_{CBO}, $V_{CE(s)}$, and h_{FE} parameter values among the 200 units after 1000 hours and at the end of 2000 hours of the Storage Life (Group C) test. A photograph of mounted and unmounted 2N699 transistors adjacent to a pencil eraser is included as Figure 2-4.

All of the 200 units complied with the Electrical Performance (Group A) test, parameters of RCA Specification A-8948874, Revision B. There were no failures among the units subjected to the three parts of the Environmental Test (Group B) test. Measurements made after the 2000 hour (Group C) Storage Life Test indicate that two of the 200 units were degradational failures in regard to the I_{CBO} parameter.

In addition to the above tests, environmental test data on the transistor families used for the RCA program are included. These data were obtained under conditions which equal or exceed the requirements of RCA Group B and Group C tests.

3.3.4 CORRELATION OF DATA

During the 2N697 program preceding this project, a considerable effort was expended at Rheem and at the glass-to-metal seal vendors' plants in attempting to establish the minimum seal length possible in mass production for reliable parts. Initially, seals from .015" to .045" were made in the laboratory at Rheem and at ITT Farnsworth. Glass cracking and leaks led to a decision, early in the development, to consider nothing under a .035" seal length (header height). After more than one hundred thousand units had been manufactured and tested, it was the belief of Zell Products that the .035" header could be produced reliably. However, in view of the reliability requirements of the program, it was jointly decided by representatives of RCA, the Signal Corps, Zell Products and Rheem Semiconductor that a .045" header would remove all doubt about the seal integrity. At this point, the present program for the 2N699 transistor microelement was started. Subsequent tests of .045" headers indicated that units with this header thickness could be processed in the same manner as the standard TO-5 or TO-18 packages.

Long term, 200°C, storage tests at RCA produced some opens which were due to bond failures. Approximately 400 units were returned to Rheem for analysis. In September, 1961, a program was started to improve the bond strength. The results and the data for this program are described on pages of Section V of this report.

As a result of this program, all microbloc device production has been converted to the new wedge bonding technique.

TABLE 2-1

GROUP A TEST REQUIREMENTS FOR MICROELEMENT 2N699 TRANSISTORS

(Pertinent Specification A-8948874, Revision B)

Test	Conditions	Sym.	Min.	Max.	Unit
(Group A) Collector cut-off current	V_{CB} = 60 I_E = 0	I_{CBO}	-	1	uAdc
Collector-emitter voltage	I_{CER} = 100 ma R_{BE} = 10 ohms PW = 167 usec duty cycle = 1%	LV_{CER}	80	-	Vdc
Collector-emitter saturation voltage	I_C = 150 ma I_B = 15 ma	$V_{CE(Sat)}$	-	4	Vdc
Base-emitter saturation voltage	I_G = 150 ma I_B = 15 ma	$V_{BE(Sat)}$	-	1.3	Vdc
Small Signal current gain at f = 20 mc	I_C = 50 ma V_{CE} = 10 volts	h_{fe}	2.5	-	
DC pulse current gain	I_C = 150 ma V_{CE} = 10 volts PW = 12 usec duty cycle = 2%	h_{FE}	40	-	
Switching time (See test circuit, Figures 1 and 2)	I_C = 150 ma V_{CC} = 7 volts I_{B1} = I_{B2} = 15 ma PW = 8 usec duty cycle = 2%	td + tr ts + tf	- -	300 900	usec usec
Output capacitance	I_E = 0 V_{CB} = 10 volts	C_{ob}	-	20	uuf
Collector cut-off current at 125°C	V_{CB} = 60 volts I_E = 0 T_A = 125° ± 3°C	I_{CBO}	-	100	uAdc
Thermal resistance (See 4.1.3)	T_j = 200°C	j-c	-	75	deg. C/W

TABLE 2-2
ANALYSIS OF ENVIRONMENTAL (GROUP B) TESTS

SUB-GROUP	TEST AND SPECIFICATION
I	a. Thermal Shock - 107 of MIL-STD-202A, Cond. A b. Moisture Resistance - 106A of MIL-STD-202A, 10 cycles
II	a. Centrifuge - 40.4 of MIL-S-19500B (20,000 g's) b. Vibration - 204 of MIL-STD-202A, Cond. C, (non-operating)
III	a. Shock - conforms with 202A of MIL-STD-202A, 500 g

TYPE TESTED
2N699 B6
SPECIFICATION
A-8948874, Rev. B.
DATE ISSUED (Spec)
6 June 1962

SUB-GROUP	ENVIRONMENTAL CONDITIONS
I	a. 5 cycles at -55°C, 30 min.; 25°C, 10 min.; 85°C, 30 min.; 25°C, 10 min. b. Ten 24 hour cycles variable temperature (25 to 65°C) relative humidity (90 to 95%)
II	a. 4 Orientations, one minute duration at 20,000 g b. 2 hours in each of 3 orientations, .06" max. 10-55-10 cps in 1.0 min. and 55 to 2000 cps in 35 ±5 minutes in 3 orientations
III	a. 5 blows at 500 g minimum; 1.0 milliseconds duration in each of four orientations, X_1, X_2, Y_1, Y_2 (Total 20 blows)

FAILURE ANALYSIS

SAMPLE SIZE	SUB-GROUP	FAILURES	CLASSIFICATION OF FAILURES
10	I	0	
10	II	0	
10	III	0	

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS	INITIAL LIMITS		POST TEST LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	V_{CB} = 60 V I_E = 0		1.0μA		1.2μA		1.2μA
h_{FE}	V_{CE} = 10 V I_C = 150 ma PW = 12 μsec Duty cycle = 2%	40		32		32	
$V_{CE(sat)}$	I_C = 150 ma I_B = 15 ma		4.0Vdc		4.5Vdc		4.5 Vdc

TABLE 2-3
FAILURE RATE AND ANALYSIS OF C TESTS

TYPE	TESTED
2N699	B6
SPECIFICATION	REV
A-8948874	B
MFG.	
RHEEM	
DATE ISSUED (Spec)	
6 June 62	

FAILURE RATE

ENVIRONMENT	DEGRADATIONAL		INOPERABLE	
	MTBF	FRACTION DEF.	MTBF	FRACTION DEF.
Storage Life 2000 hrs @200°C	127,000 (60% confidence)	.0078 per 1000 hrs	437,000	.0023 per 1000 hrs

FAILURE ANALYSIS

SAMPLE SIZE	TO TOTAL HOURS	FAILURES	250 HOUR FAILURES	1000 HOUR FAILURES	2000 HOUR FAILURES
200	400,000	I_{CBO} – 2	–	0	2
		h_{FE} – 0	–	0	0
		$V_{CE(sat)}$ – 0	–	0	0

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS	INITIAL LIMITS		END OF LIFE LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	V_{CB} = 60V I_E = 0	–	1.0 μA.	–	1.2 μA.	–	1.2 μA.
h_{FE}	I_C = 150 ma V_{CE} = 10 V PW = 12 μsec duty cycle $\leq$ 2%	40	–	32	–	32	–
$V_{CE(sat)}$	I_C = 150 ma I_B = 15 ma	–	4.0Vdc	–	4.5Vdc	–	4.5Vdc

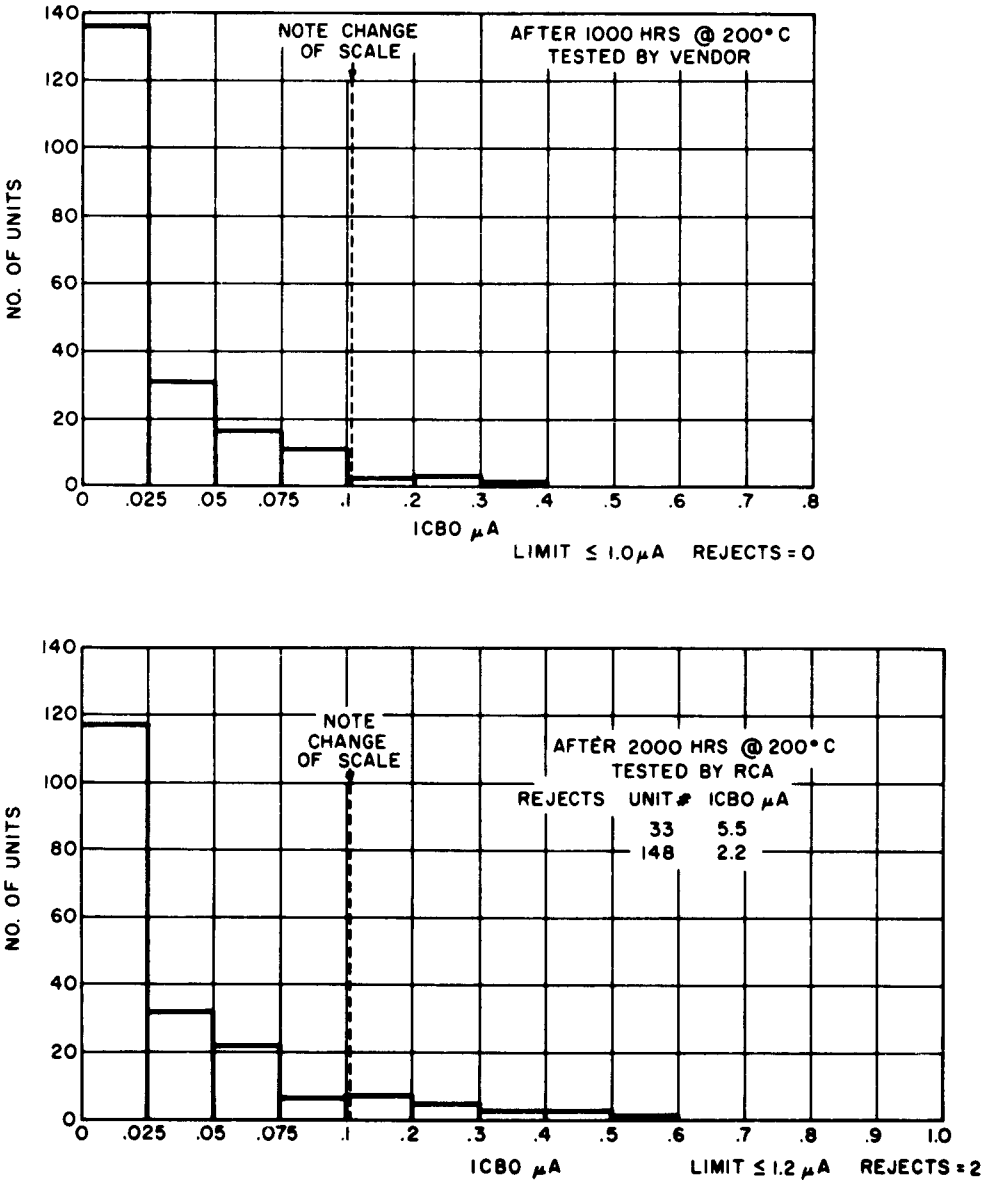
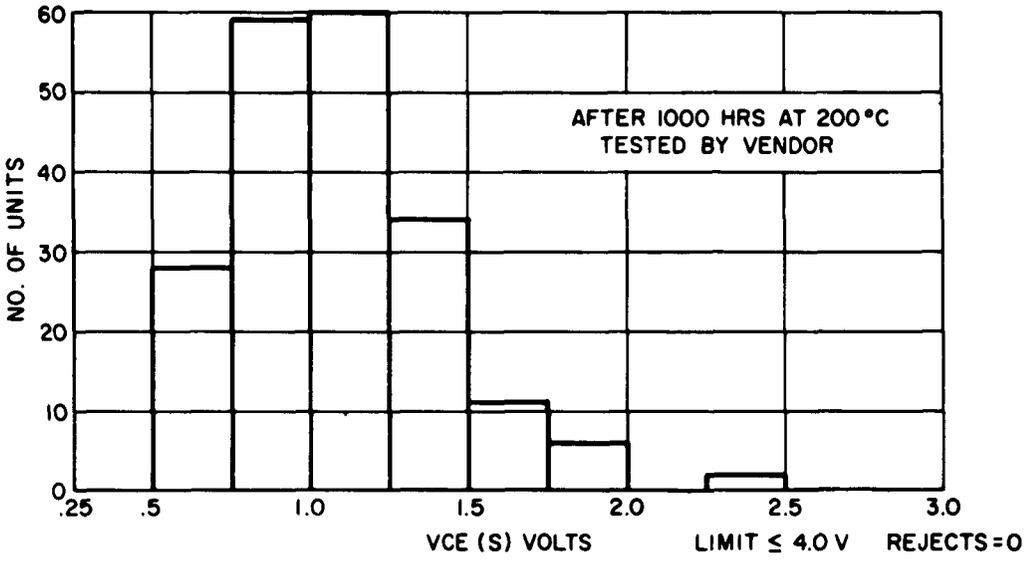


Figure 2-1. Storage Life Tests of I_{CBO} for 200 Rheem 2N699 Microelement Transistors TA = 25°C, V_{CB} = 60 v, I_E = 0



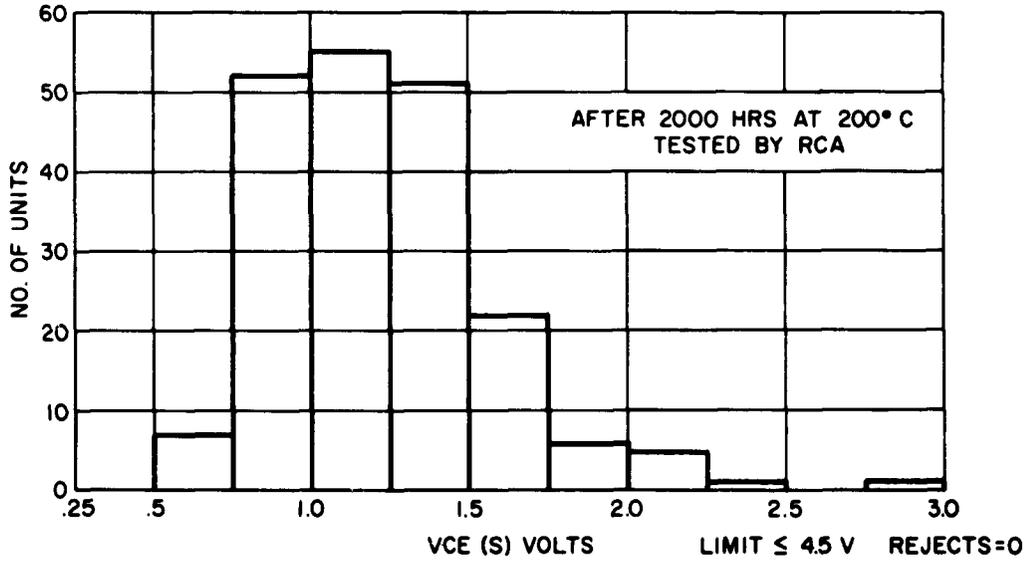
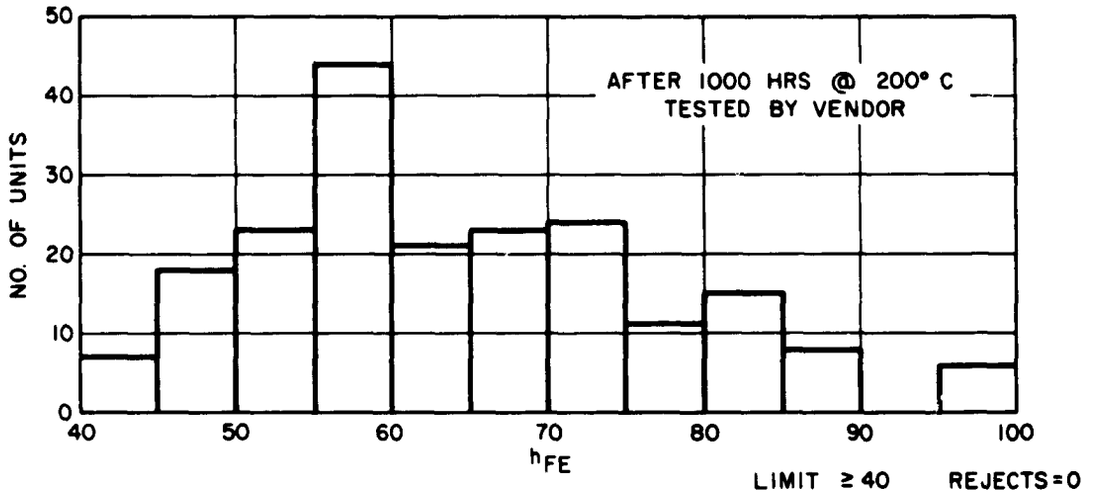


Figure 2-2. Storage Life Tests of $V_{CE(S)}$ for 200 Rheem 2N699 Microelement Transistors TA=25°C, I_C=150 ma, I_B=15 ma



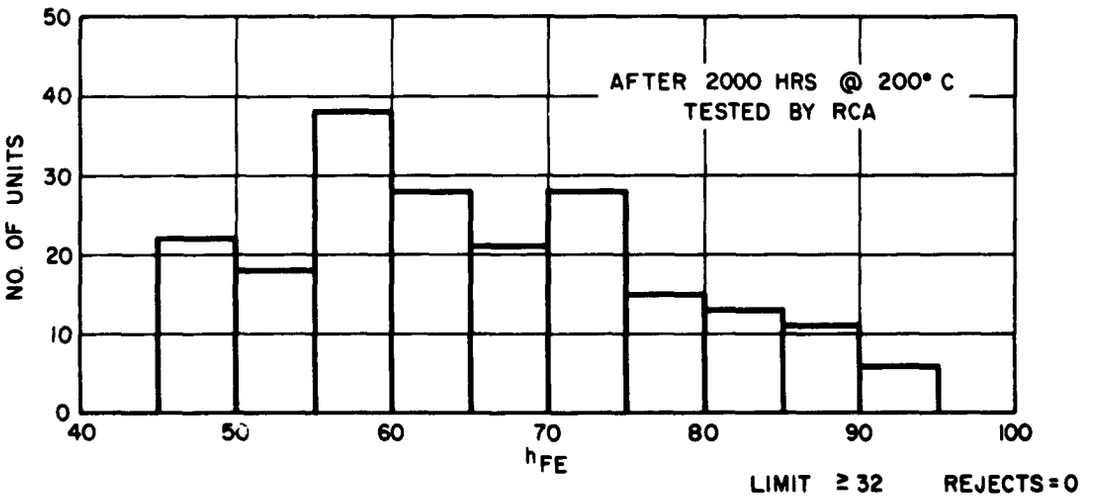


Figure 2-3. Storage Life Tests of h_{FE} for 200 Rheem 2N699 Microelement Transistors TA=25°C, V_{CE}=10 v, I_C=150 ma

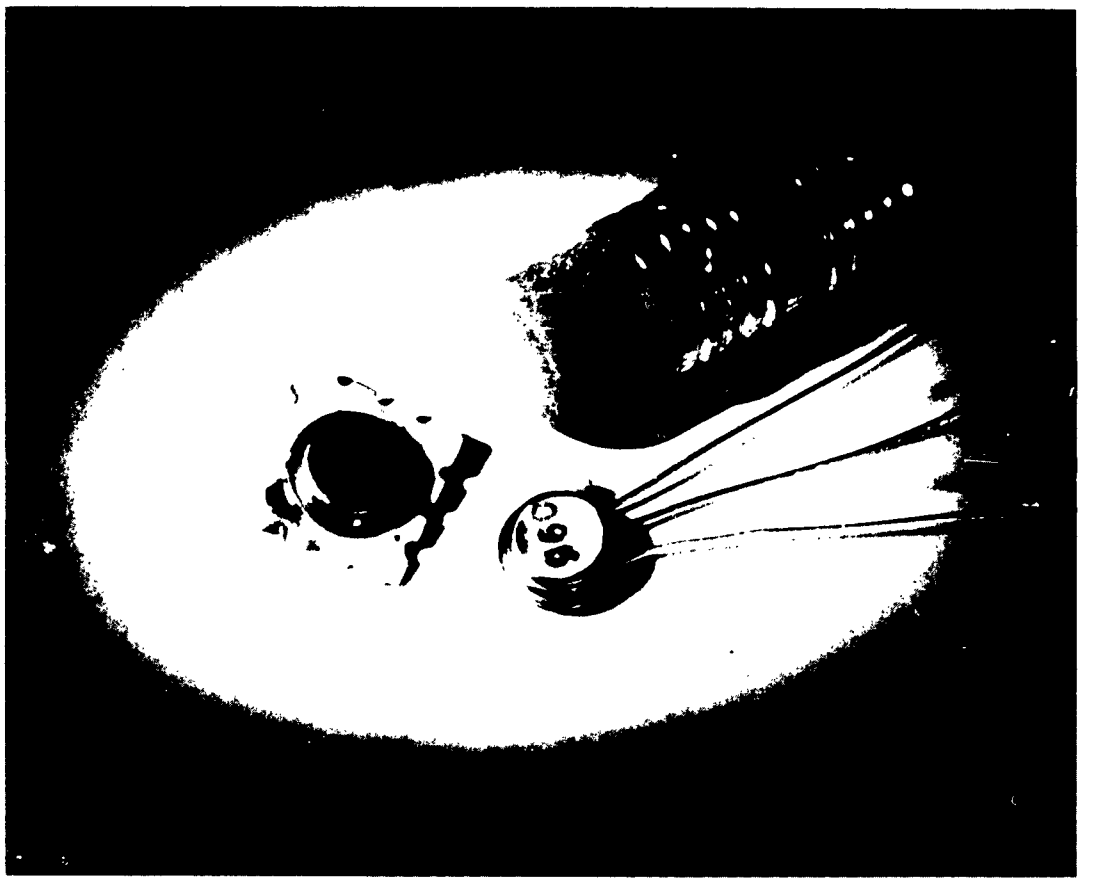


Figure 2-4. Rheem 2N699 Transistor of Task 18-2 (Magnification: 5x), Adjacent to Eraser end of a Drawing Pencil

3.4 UNIT SPECIFICATIONS

The specifications in effect during this project, per paragraph 2.1 on either specification, were:

RCA Dwg. A-8978123 Hermetic Package for Micro Transistor

RCA Dwg. A-8972091 Gen'l. Specification for Micro Transistor

RCA Dwg. A-8948874 Medium Speed High Voltage Transistor

Data in Appendices A and B indicate our conformance to all specified requirements.

3.5 PRODUCT EVALUATION

Since the final design uses the TO-18 diameter and lead circle, it is compatible with existing device packaging equipment in the industry. The use of a Kovar-glass seal and resistance welded closure has long been considered the most reliable closure for electron devices. This development has resulted in a package of the smallest possible height commensurate with the reliability requirements and the present state-of-the-art. The improvements in lead bonding, made during this program, are a substantial contribution and a necessity to the art of packaging devices for space restricted applications.

3.6 DELIVERY

2N699 Delivery Schedule

	Qty.	Contract Date	Qty.	Actual Date
	15	1-25-61	15	1-25-61
	85	3- 1-61	85	2-21-61
	200	3-31-61	200	3-31-61
Total	300		300	

NOTE: Replacement shipment of 200 - 2N699 units was made on March 28, 1962.

4. CONCLUSIONS AND RECOMMENDATIONS

As a result of the work herein described, it has been concluded:

(1) that .043" is a minimum nominal seal length for headers of this type for the present state-of-the-art of glass-to-metal sealing and semiconductor processing;

(2) that .065" is a minimum nominal height for axial lead packages for collector mounted devices of these types; and

(3) that the package is fully as reliable as the conventional TO-18 or TO-5 configurations.

SECTION III

FORMAL ENGINEERING REPORT
ON
MICROELEMENT 2N1132 TRANSISTOR, TYPE B-5
TASK 18-3
MICRO-MODULE PROGRAM EXTENSION I

PO GX1-946255-7160-24-D38

FAIRCHILD SEMICONDUCTOR
545 WHISMAN ROAD
MOUNTAIN VIEW, CALIFORNIA

November 15, 1962

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. PURPOSE OF TASK 18-3

Fairchild Semiconductor was awarded a contract from Defense Electronic Products of the Radio Corporation of America at Camden, New Jersey to repackage the 2N1132 Silicon Mesa Transistor into a smaller semiconductor package suitable for mounting on Micro-Module wafers. The repackaging of this device must not degrade it from the high reliability of the device as encased in the JEDEC (TO-18) package.

2. ABSTRACT

A new semiconductor package has been developed based on the outline dimensions of the JEDEC TO-18 with the following exceptions; the package height was decreased from 0.205 inches maximum to 0.065 inches maximum, and the diameter of the leads was decreased from 0.017 inches to 0.012 inches nominal wire size. The package was fabricated using standard Kovar hard glass sealing techniques. To insure hermeticity and decrease thermal resistance, the header was constructed using a solid Kovar slug. A thermal resistance of 43.7°C per watt, measured from junction to heat sink, has been established for this package, containing a 2N1132 transistor. The TO-18 pin circle of 0.100 inches diameter and flange diameter of 0.210 inches were unchanged in the new package; this factor made possible the assembly of the package with existing assembly equipment. The engineering effort could therefore be concentrated on the package because of the elimination of the need for expensive large scale modifications to equipment and tooling necessary to accommodate the package. The development of the package by Fairchild was completed in March 1961. On April 18, 1962 the new package was standardized as the JEDEC TO-46.

Evaluation tests were conducted on the 2N1132 device encapsulated in the JEDEC TO-46 package. The transistors were subjected to storage life tests consisting of aging for 1,000 hours at 200°C and to environmental life tests consisting of temperature cycling, moisture resistance, constant centripetal acceleration, vibration fatigue, and shock. All tests were conducted in accordance with MIL-S-19500B, the RCA Specifications and the Purchase Order. The reliability of the 2N1132 encapsulated in the JEDEC TO-46 has been well established, as there were no failures in any of the tests performed on these transistors. Figure 3-1 displays the construction techniques used in fabricating the 2N1132 transistor.

3. NARRATIVE AND DATA

3.1 DESIGN CONSIDERATIONS

It was specified that the package should be constructed using normal glass-to-metal sealing procedures, and that closure be made using resistance welding techniques. The package retained the flange diameter, pin circle diameter and flange thickness of the JEDEC TO-18 package. The header was fabricated from a coined Kovar slug. The Kovar lead diameter was decreased from 0.017 inches to 0.012 inches, nominal wire size. The thickness of the header was originally established at 0.035 inches; but was

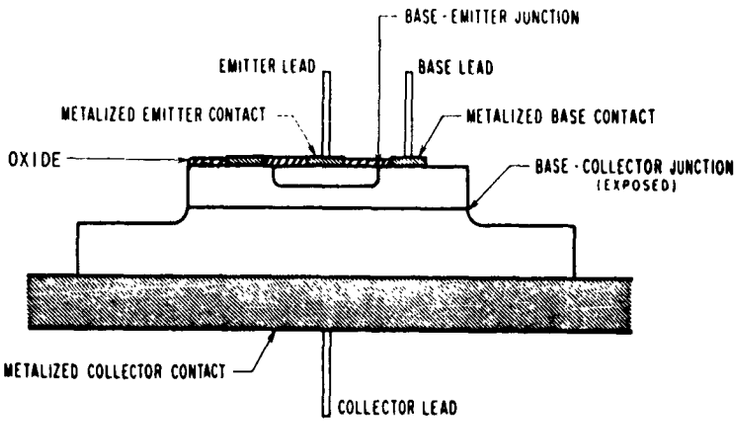


Figure 3-1. Double Diffused Mesa Transistor, 2N1132

later increased to 0.045 inches to insure a hermetic seal. The headers were purchased from Veritron West Inc., of North Hollywood, California, an outside manufacturer of glass-to-metal seals. The can was stamped from electronic Grade A nickel. This material was selected because of its weldability and corrosion resistance properties. Figures 1-2 and 1-3 of Section I are drawings of the header and can.

3.2 FABRICATION PROCEDURES AND EQUIPMENT

3.2.1 DESCRIPTION OF PROCESS

The procedures used to assemble and encapsulate the 2N1132 transistor in the TO-46 package do not differ from the methods used to encapsulate the same device in the JEDEC TO-18 package. The Process Flow Chart (Figure 1-4, Section I) displays the sequence of operation.

All materials and supplies used for assembly of the packages were inspected by the Quality Assurance Department prior to their release to the assembly line. Lot numbers and vendor identification were maintained on all material released to the assembly lines.

Electrically and visually sorted 2N1132 dice were inventoried prior to assembly; lot identification was maintained through all assembly operations to insure adequate feed back of information to the processing and diffusion sections.

The first assembly operation was the bonding of the die to the header using a gold silicon eutectic as the bonding agent. The assembly was heated to 385°C to perform this operation. The gold emitter and base leads were then bonded to the aluminum patterns of the die. The assembly was heated to 340°C and the leads were bonded by thermal compression to the gold using a pyrex capillary. The emitter and base leads were then welded to the header pins by the use of welding techniques involving a capacitor dc discharge.

Random samples were inspected from each of the previous assembly operations by the Quality Assurance Department, and individual operator performance records were maintained. These records were posted to enable each operator to observe her own performance.

The transistor subassemblies were then washed with heated, deionized, distilled water and baked dry to remove any contaminants. The subassemblies were vacuum baked at 300°C at a pressure of 5×10^{-6} mm of Hg for three hours. The transistors were encapsulated and welded in an inert, controlled atmosphere. The moisture content of the nitrogen atmosphere in the dry box was continually monitored and at no time was allowed to exceed 120 ppm. Sample units were visually inspected and helium leak tested to insure proper welding.

All welded transistors were then subjected to environmental tests consisting of Drop Test, Temperature Cycle, Centrifuge and pressure tests. These tests were performed in accordance with MIL-S-19500B. The transistors were aged for 1,000 hours at 200°C to increase stability.

The transistors were electrically tested to the RCA specifications. The test equipment was programmed by the Electronic Maintenance Section. All electrical equipment was rechecked every four hours to insure proper programming. All electronic equipment and meters were calibrated against standard maintained by the Calibration Section.

Maintenance and calibration logs were maintained on all electronic equipment. All reject transistors were sent to Quality Assurance for Reject Analysis.

Random samples from each lot of tested transistors were taken by the Quality Assurance Department. These samples were retested to insure compliance with the specifications. These samples were not tested on production test equipment.

The transistors were tested in accordance with MIL-S-19500B to insure hermeticity.

The transistors were then subjected to the Storage Life and Environmental Tests specified by RCA. All tests were conducted in accordance with MIL-S-19500, the RCA Specifications, and the Purchase Order.

After testing, the transistors were marked, packed and processed for shipment.

3.2.2 and 3.2.3 EQUIPMENT AND EVALUATION

The TO-46 assembly equipment used in fabricating the 2N1132 transistor is identical with that described in paragraphs 3.2.2 and 3.2.3 of Section I.

3.3 TEST PERFORMANCE AND DATA

3.3.1 DESCRIPTION AND PURPOSE OF TESTS

After successfully withstanding electrical testing in accordance with the (Group A Test) requirements of Table 3-1 the transistors were subjected to Storage Life Tests and Environmental Tests. The transistors to be used in the Environmental Test were random samples taken from the lot. The remainder of the units were used in the Storage Life Tests. The Storage Life Tests consisted of aging for 1,000 hours at 200°C. The degradation and inoperable limits were defined and the failure rates for each condition were computed as Mean Time between Failures, and Fraction Defective per 1,000 hours. Distribution and stability of the parameters were plotted. The Environmental Tests consisted of three parts, Glass Seal Characteristics, Dynamic Characteristics, and Shock.

3.3.2 ANALYSIS OF PERFORMANCE DATA

A complete analysis of the tests performed as well as the data acquired for each parameter was compiled in two sections. The first section contains the analysis obtained from the Storage Life Tests, the second section contains the analysis obtained from the Environmental Tests.

3.3.3 STORAGE LIFT TESTS

This section is an account of Storage Life testing at 200°C. This test was performed in accordance with paragraphs 40.7, 40.7.1 and 40.7.1.1 of MIL-S-19500B.

Both degradational and inoperable limits are defined and the failure rates for each condition are computed as Mean Time Between Failures and Fraction Defective per 1,000 hours in Table 3-2.

To complete the presentation, both the distribution and stability of the test parameters are plotted in Figures 3-2, 3-3, and 3-4. For parameter stability the charts show the changes in the test parameters from their initial readings.

TABLE 3-1
GROUP "A" TEST REQUIREMENTS

(RCA DWG. A-8978121 Revision C, dated 27 November 1961)

Test	Measurements Acceptance Tests				
	Conditions	Sym.	Min.	Max.	Unit
Collector cut-off current	V_{CB} = -30 I_E = 0	I_{CBO}		-1	μAdc
Collector-base breakdown voltage	I_C = -100 u I_E = 0	BV_{CBO}	-50		Vdc
Collector-emitter voltage (Note 1)	R_{BE} = 10 ohms I_C = -100 ma (pulse) P_W = -167μsec Duty cycle 1%	LV_{CER}	-50	V	Vdc
Emitter cut-off current	V_{EB} = -5 I_C = 0	I_{EBO}		-100	μAdc
Base-emitter saturation voltage	I_C = 150 ma I_B = 8.5 ma	V_{BE} (sat)		-1.5	Vdc
Collector-emitter saturation voltage at 125°C	I_C = 150 ma I_B = 8.5 ma	V_{ce} (sat)		4.2	Vdc
Small signal current gain at f = 20 mc	I_C = 50 ma V_C = -10V	h_{fe}	2.0		
DC pulse current gain at -55°C	I_C = 150 ma V_C = -4V P_W = -8μsec Duty Cycle 20%	h_{FE}	15		

TABLE 3-1 (Continued)
GROUP "A" TEST REQUIREMENTS

Test	Measurements Acceptance Tests				
	Conditions	Sym.	Min.	Max. ρ	Unit
Switching times (see Figure 1 for test circuit)	I_C = 150 ma V_{CC} = -7V P_W = 8 μsec I_{B1} = I_{B2} = -15ma Duty cycle 20%	$t_d + t_r$ $t_s + t_f$		150 600	μsec μsec
Output capacitance	V_C = -10 I_E = 0	C_{ob}		45	$\mu\mu$f
Collector cut-off current	V_{CB} = -30V I_E = 0 T_A = 125° ±3°C	I_{CBO}		-200	μAdc
Emitter cut-off	V_{EB} = -5 I_C = 0 T_A = 125°C ±3°C			-800	μAdc
Thermal Resistance (see Figure 3)	T_j = 200°C	O_{j-c}		75	°C/watt

Note 1: LV_{CER} is increased to 40V or until I_{CER} = 100ma. I_{CER} must be less than 100ma with LV_{CER} = 40V.

There was no failure for $V_{CE(SAT)}$. In order to secure additional information quantities of known rejects were subjected to Life Tests. The primary purpose of testing rejects was to determine whether further degradation would occur. A quantity of 17 marginal units (h_{FE} not within specifications) were placed on life tests. At the end of 1,000 hours five of these transistors were within limits. Of the 183 good units before life, all were good after 1,000 hours. Three marginal units in respect to $V_{CE(SAT)}$ parameter were subjected to life tests. After 1,000 hours the three units were still beyond specified limits. An additional 197 transistors were all within specifications before life tests. Of this quantity, one failure for $V_{CE(SAT)}$ occurred after 1,000 hours of storage life test at 200°C.

TABLE 3-2
ANALYSIS OF STORAGE LIFE (GROUP C) TEST

FAILURE RATE

ENVIRONMENT	DEGRADATION		INOPERABLE	
	MTBF	FRACTION DEF.	MTBF	FRACTION DEF.
200°C Storage Life 1000 hrs	99,000	.0101 per 1000 hrs	216,000	.0046 per 1000 hrs

TYPE TESTED
2N1132 B5
SPECIFICATION
A-8978121 Rev. C
DATE ISSUED
7 November 1962

FAILURE ANALYSIS

SAMPLE SIZE	TOTAL HOURS	FAILURES (Degradation)	PARAMETER	INITIAL FAILURES	1000 HOUR FAILURES
300	1,000	0	I_{CBO}	0	0
200	1,000	0	h_{FE}	17*	12
200	1,000	1	$V_{CE(sat)}$	3*	4

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS	INITIAL LIMITS		END OF LIFE LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	$V_{CB} = -30V$	–	−1.2	–	−1.2	–	−1.2
h_{FE}	$V_{CE} = -4V$ $I_C = 150ma$ PW $= 8\mu sec$ Duty cycle 20%	15 (−55°C)	–	25	–	25	–
$V_{CE(sat)}$	$I_C = 150ma$ $I_B = 8.5ma$ $T_A = 125°C$	–	4.2	–	4.4	–	4.4

*Marginal rejects for h_{FE} and $V_{CE(sat)}$ were placed in life test to make up the 200 sample size and determine what further degradation would occur. Of the 17 rejects for h_{FE} 5 were within specified limits after 1,000 hours and no additional failures occurred during 1,000 hour life test. There were 3 $V_{CE(sat)}$ rejects, initially. These plus 1 degradational failure were still rejects at the end of life tests.

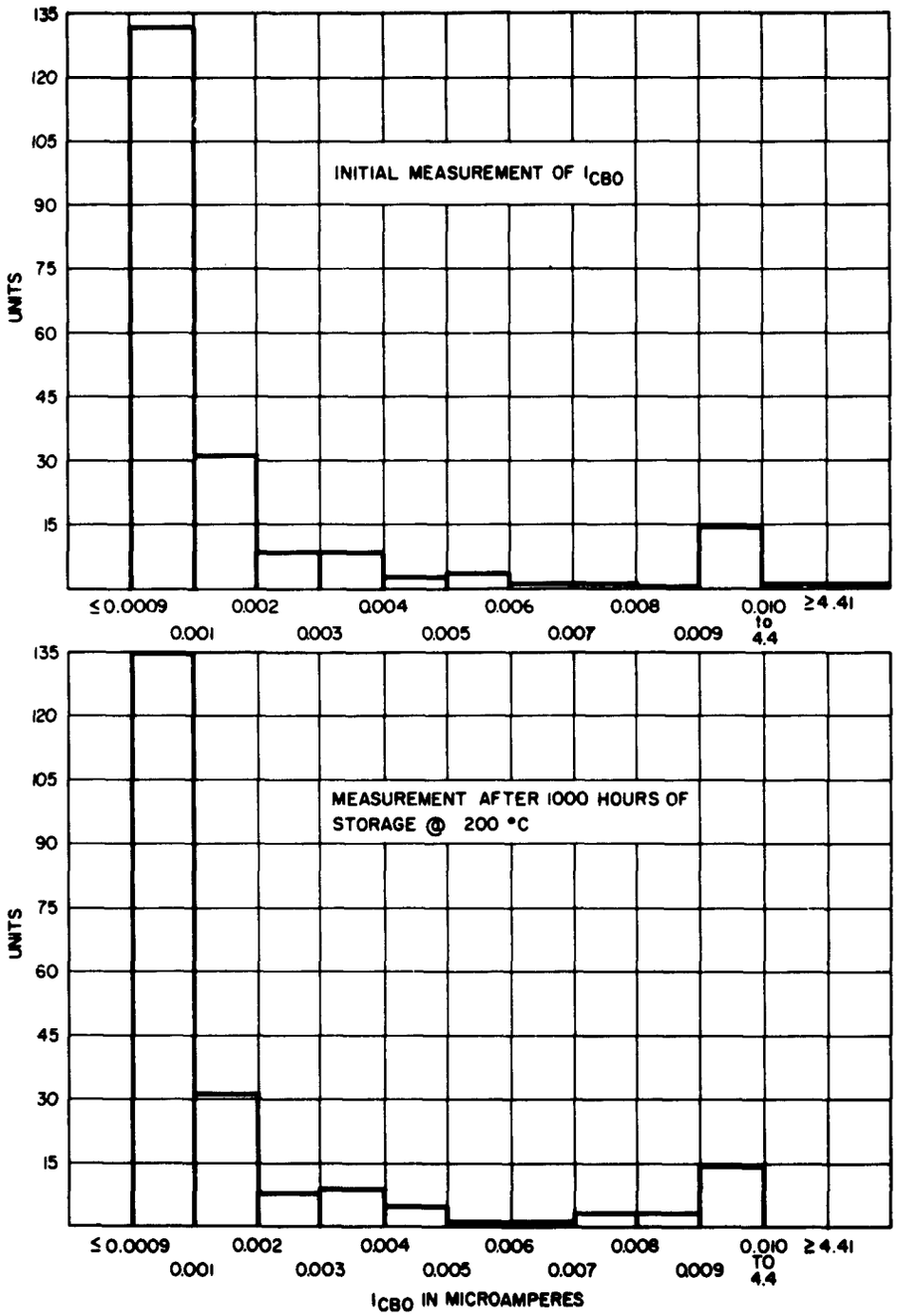


Figure 3-2. Parameter Distribution, — Units vs. I_{CBO} for 200 Fairchild 2N1132 (Type B-5) Transistors

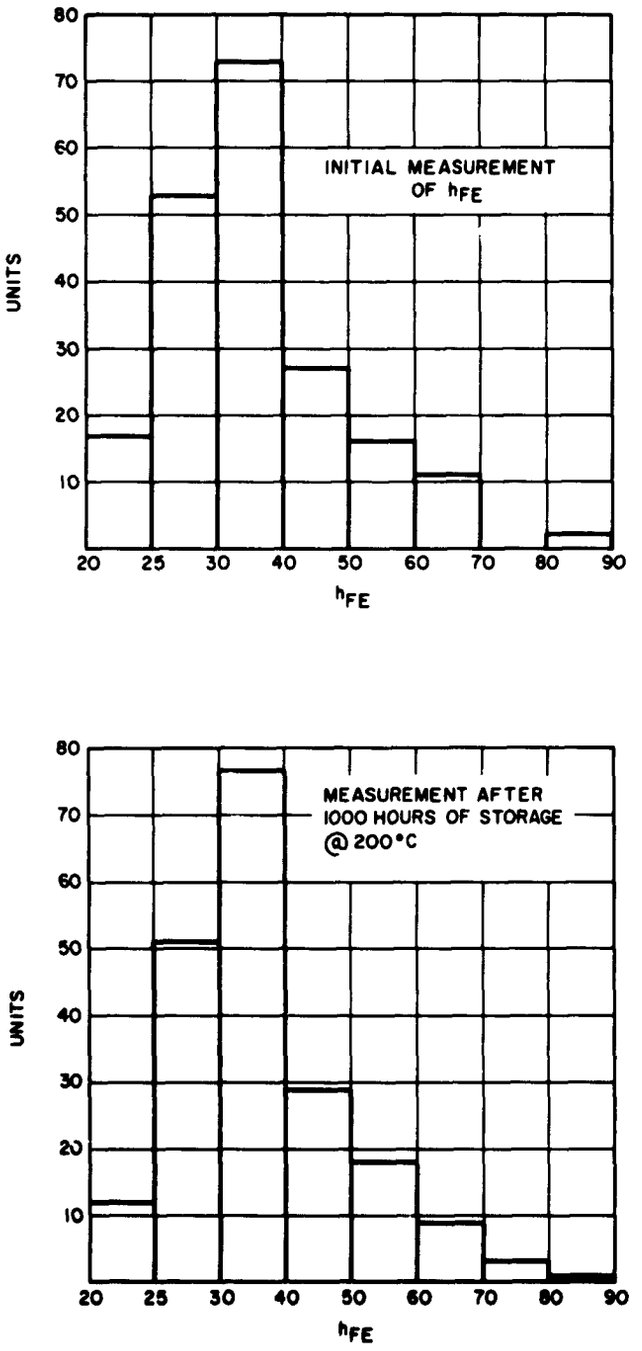
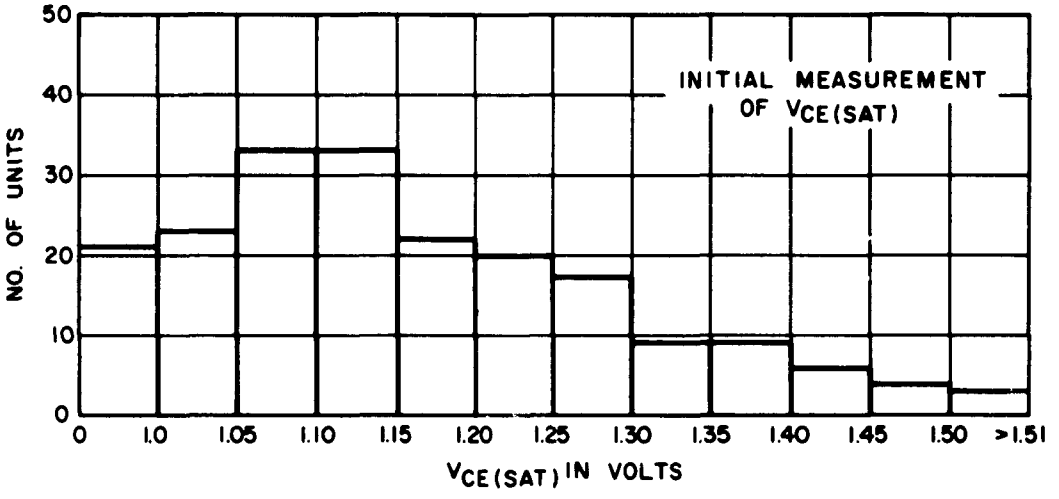


Figure 3-3. Parameter Distribution, — Units vs. h_{FE} for 200 Fairchild 2N1132 (Type B-5) Transistors



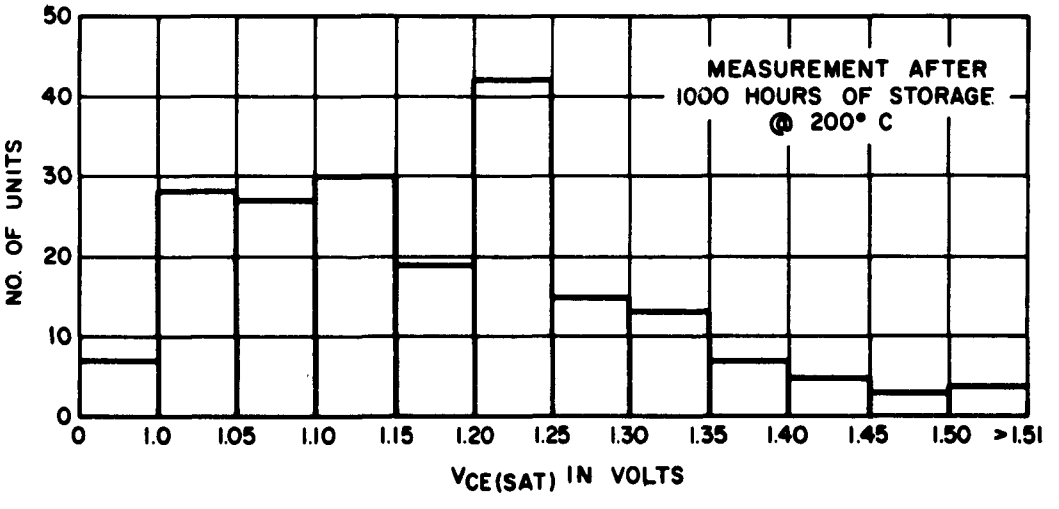


Figure 3-4. Parameter Distribution, — Units vs. $V_{CE(SAT)}$ for 200 Fairchild 2N1132 (Type B-5) Transistors

As a result of life testing, there was one failure for all the parameters. This is well within the number of such failures permitted by the specification.

3.3.4 ENVIRONMENTAL TEST

For the Environmental Tests on the devices produced under Task 18-3 test samples were selected at random from the lot. All such tests were performed in accordance with MIL-S-19500B. The same initial and post test limits were used here as were used for Life Tests.

The Environmental, or Group B, Tests are described as follows: During Subgroup I, testing for glass seal characteristics, - all units were checked for moisture resistance, and were temperature cycled. During Subgroup II, - testing for dynamic characteristics, - the units were subjected to constant (centripetal) acceleration and fatigue. Testing is completed with Subgroup III, - a shock test.

The details of these tests and an analysis are found in Table 3-3.

There were no failures as a result of thest tests.

3.4 UNIT SPECIFICATIONS

The transistors were physically and electrically tested in accordance with the following specifications:

RCA dwg. A-8978123 Hermetic Package for Microelement Transistors

RCA dwg. A-8978121 General Specifications for Microelement Transistors

RCA dwg. A-8948865 Type B-5 Transistors

The information contained in 3.3.3 and 3.3.4, above, indicate Fairchild's conformance to all the specification requirements. The electrical specifications were much more stringent than the EIA specifications for a 2N1132.

3.5 PRODUCT EVALUATION

In large production quantities, assembly and encapsulation of the 2N1132 transistor in the JEDEC TO-46 package can be accomplished at a cost approximating the assembly costs of the same transistors in the JEDEC TO-18 package. The technical advances in assembly tooling and automation will be applicable to the assembly of both packages. These factors contribute to a much lower manufacturing cost, and eliminate duplication of equipment. Figure 3-5 is a photograph of the 2N1132, both unmounted and mounted, adjacent to a dime for size comparison.

TABLE 3-3
ENVIRONMENTAL TEST ANALYSIS — "B" TESTS

SUB-GROUP	TEST AND SPECIFICATION
I	a. Thermal Shock - 107 of MIL-STD-202A, Cond. A. b. Moisture Resistance - 105A of MIL-STD-202A, 10 cycles.
II	a. Centrifuge - 40.4 of MIL-S-19500B (20,000 g). b. Vibration - 204 of MIL-STD-202A, Cond. C, (non-operating)
III	a. Shock - conforming to 202A of MIL-STD-202A, 500 g.

TYPE TESTED 2N697 B-4
SPECIFICATION A-8978122, Rev. C
DATE ISSUED (Spec) 19 March 1962

SUB-GROUP	ENVIRONMENTAL CONDITIONS
I	a. 5 cycles at -55°C, 30 min.; 25°C, 10 min.; 85°C, 30 min.; 25°C 10 min. b. Ten 24 hour cycles variable temperature (25 to 65°C) relative humidity (90 - 95%)
II	a. 4 orientations, one minute duration at 20,000 g. b. 2 hours in each of 3 orientations .06" max. 10-55-10 cps in 1.0 min. and 55 to 2000 cps in 35 ±5 minutes in 3 orientations.
III	a. 5 blows at 500 g minimum, 1.0 milliseconds duration in each of four orientations X_1, X_2, Y_1, Y_2, (Total 20 blows).

FAILURE ANALYSIS

SAMPLE SIZE	SUB-GROUP	FAILURES	CLASSIFICATION OF FAILURES
10	I	0	
6	II	0	
6	III	0	

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS TA = 25°C	INITIAL LIMITS		POST TEST LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	V_{CB} = 30v I_E = 0		1.0μA		1.2μA		1.2μA
h_{FE}	I_C = 250 ma V_{CE} = 4v P_W = 8μsec Duty Cycle = 20%	19		17.5		17.5	
$V_{CE(sat)}$	I_C = 250ma,, I_B = 15 ma PW = 300μsec T_A = 125°C Duty Cycle ≤ 2.0%		4.2Vdc		4.4Vdc		4.4Vdc

Figure 3-5. Fairchild 2N1132 Transistor of Task 18-3 Adjacent to a Dime for Size Comparison

3.6 DELIVERY

The delivery schedule of transistors shipped to RCA is as shown below:

Quantity Required	Date Required	Quantity Shipped	Date Shipped	Use of Transistors
50	12-1-60	50	12-14-60	Signal Corps Tests
100	1-1-61	100	1-18-61	Hermeticity Tests
50	2-1-61	50	2-6-61	Signal Corps Tests
150	2-1-61	22	2-6-61	"B" Tests
200	7-1-61	150	8-24-61	2000 Hr. Tests
		50	9-7-61	
100	8-1-61	100	9-7-61	Signal Corps Tests

4. CONCLUSIONS AND RECOMMENDATIONS

4.1 CONCLUSIONS

It was concluded that a minimum seal length of 0.042 inches is necessary to insure a hermetic seal of the leads with present glass to metal seal technology. It was concluded that thermal compression bonding of the lead wires to the posts is not favorable and that a resistance weld must be effected to insure high reliability. It was concluded by the tests conducted that the Fairchild 2N1132 device encapsulated in the JEDEC TO-46 package is a reliable transistor.

4.2 RECOMMENDATIONS

The tests were conducted on a relatively small number of transistors, and even though there were no failures as a result of any of the tests conducted; it is recommended that similar tests be conducted on a sufficiently large number of transistors to support these findings.

SECTION V

FORMAL ENGINEERING REPORT
ON
MICROELEMENT 2N697 TRANSISTOR, TYPE B-4
TASK 18-5
MICRO-MODULE PROGRAM EXTENSION I

PO GX1-946253-5773-24-D38

RHEEM SEMICONDUCTOR OPERATION OF RAYTHEON CO.
MOUNTAIN VIEW, CALIFORNIA

August 15, 1962

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. PURPOSE OF TASK 18-5

The purpose of this contract was to design and supply test units and test data of 2N697 transistors in packages suitable for mounting on Micro-Module wafers and with electrical environmental and mechanical properties as described in Task 18-5 and pursuant Rheem and RCA proposals, correspondence and purchase orders.

2. ABSTRACT

A micro-element transistor package has been developed using state-of-the-art package fabrication techniques and materials. The required 2N697 transistors have been enclosed and tested in this package to RCA specifications referred to in Task 18-5, and the results indicate that the development has resulted in a highly reliable unit.

Kovar-hard glass seals and resistance welding for final closure were selected as the established techniques for dependable encapsulation. Using these materials, an effort was made to determine the design that would meet the dual requirements of hermeticity and minimum package height. After due analysis, the selected design, a solid Kovar slug, was fabricated in a variety of sizes, to determine minimum seal length, weld flange thickness and other height-critical parameters. It is believed that the resulting .065" nominal package height is a minimum for the present state of the art of header fabrication and semiconductor processing.

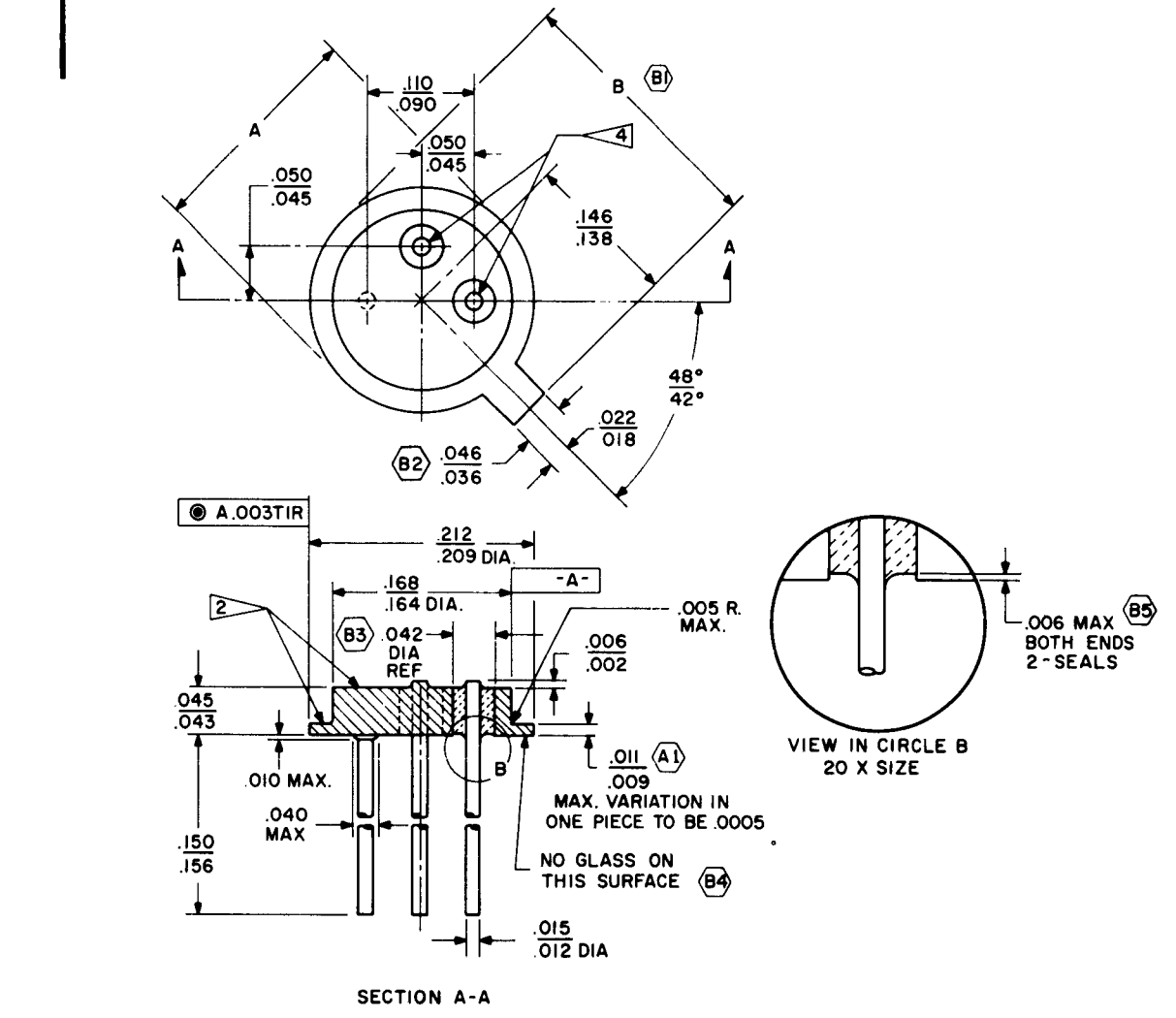
It was also necessary to improve on existing internal lead bonding procedures to provide leads that would minimize the package height requirement and at the same time stand up under centrifuge and thermal cycles.

Since lower package thermal resistance increases the reliability of any device, this factor was an important consideration. The final design has a thermal resistance of less than 50°C/watt as compared to 68°C/watt for a conventional Kovar TO-5, as measured from junction to heat sink and containing typical 2N697 type transistors.

3. NARRATIVE AND DATA

3.1 DESIGN CONSIDERATIONS

It was specified that state-of-the-art glass-to-metal sealing and resistance welding for closures be used. Per Task 18-5, Rheem Technical Proposal of May 17, 1960 and pursuant correspondence, the form factor was to be .090" maximum package height, with .050" as a desirable objective and a flange diameter equal to the TO-18 and in any case less than 0.250". Consideration of these requirements and the physical and electrical specifications indicated in the Work Statement determined the design shown in Figures 5-1 and 5-2. This is one of the designs that appeared in the Rheem Proposal and, as shown later, the final design fell within the limits indicated. Other glass-to-metal seal designs were analyzed, as discussed below, before deciding firmly on the design of Figure 5-1.

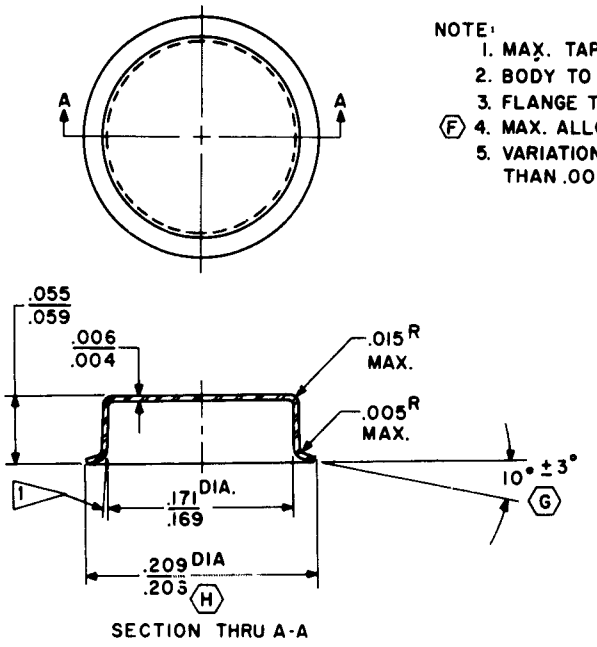


SECTION A-A

Notes:

1. Leads must be concentric to .042 ref. hole within .008 T. I. R.
2. These surfaces to be flat within .001 T. I. R.
3. Glass Rise .005 max.
4. Post top surfaces to be gold plated for thermocompression bonding, flat and free of glass.
5. Tab length to be .028 - .048 max. and will be determined by subtracting diameter "A" from dimension "B".

Figure 5-1. Microbloc Header (TO-46)



NOTE:
1. MAX. TAPER ALLOWABLE ON I.D. IS 1°. (H)
2. BODY TO FLANGE ECCENTRICITY MAX. .002 T.I.R.
3. FLANGE TO BE FLAT WITHIN .001
(F) 4. MAX. ALLOWABLE BURR ON FLANGE = .001
5. VARIATION IN FLANGE THICKNESS PER CAP NOT GREATER THAN .0005

Figure 5-2. Microbloc Header Case

Since higher heat dissipation increases reliability for a given power requirement it was felt that the design should provide for the lowest thermal resistance commensurate with the prime requirement of minimum package height.

The design of Figure 5-1 was preferred from this standpoint, compared to designs (discussed later) that provided less built-in heat transfer. Later measurements indicated the thermal resistance of this package, containing a typical 2N697 type transistor, to be less than 50°C/watt. This can be compared to 68°C/watt for the large conventional TO-5 package. This assumes that Kovar is used and in terms of the reliability requirements (Task 18) it was early decided that a Kovar-to-glass seal would be desirable.

Since the Work Statement did not restrict this development to axial leads, some consideration had to be given to radial lead configurations. Radial leads would, of course permit a lower height of package. Disadvantages, usually associated with radial leads, are: a more complex geometry which leads to the possibility of trapped contaminants, less adequate weld-flash protection, increased tooling cost, and lack of compatibility with existing assembly equipment in all semiconductor plants. In view of these disadvantages, it was decided to concentrate on axial lead approaches and the following discussion indicates why the design of Figure 5-1 was ultimately used.

Other geometries of the axial lead variety that were considered included the frying pan type, probably originated by G-E, and a low form, glass filled cup, i.e. a very flat package constructed like a conventional TO-18 header. For all axial lead designs

the header height is controlled by the glass seal length. In addition to the problems in making glass preforms and glass-to-metal seals, with small parts, there are limiting considerations such as the seal stress due to lead binding. Figure 5-3 is a section of a header through the glass seal and shows the theoretical stress pattern with the lead in lateral loading such as is the case when a lead is bent in process or during installation.

From the figure; i.e., equating moments to the areas of their respective load diagrams:*

$$q_a = \frac{6P}{a^2}\left(1 + \frac{a}{3}\right),$$

$$q_b = \frac{6P}{a^2}\left(1 + \frac{2a}{3}\right),$$

Where q_a and q_b are the maximum stress intensities; P, a load tending to bend the lead; and a, the glass seal thickness.

---

* Timoshenko, S. & D. H. Young, "Engineering Mechanics", 4th Edition, McGraw-Hill

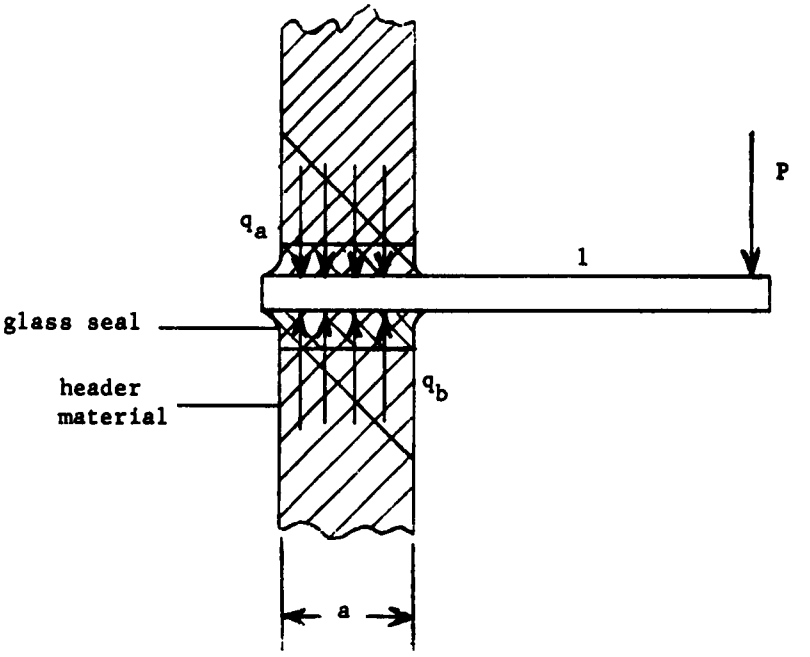


Figure 5-3

These conditions indicate that, if $2/3\ a << 1$, the maximum intensities are approximately inversely proportional to the square of the glass thickness. Also, referring to the figure, since the maximum intensity is determined by the yield strength of the lead in bending it is apparent that the lead diameter should be minimized. For actual cases, consideration should be given to the possibility that small initial glass crushing will give rise to tensile stresses. It was also realized, in considering various axial lead designs, that sufficiently thin glass seals would allow the pin to deflect as in Figure 5-4, which would stress or possibly rupture internal lead bonds. For thin glass there is also the possibility that the seal might fail in torsion at the lead-glass bond.

Deflection of the header body due to stresses during processing steps such as final sealing would also be a possible source of internal lead bond failures. This is of special importance for designs involving thin, unsupported metal eyelets, such as the "frying pan" type. This type gives a lower height package for devices mounted on vertical tabs; however, for collector-mounted devices, the total package height would be the same as for the design of Figures 5-1 and 5-2. This is so since, for the "frying pan" type, it is necessary either to elevate the device or to curve the leads to avoid shorting on the seal collars. The first alternative essentially changes the "frying pan" to the solid slug of Figure 5-1 and the second alternative is undesirable from the standpoint of mechanical stability; i. e., the leads might bend laterally, under acceleration, and short on the collars. Another feature of the design of Figure 5-1 is the protection against weld-flash which costs nothing in total package height.

These considerations eliminated the "frying pan" type of header as a possibility. The flat TO-18 type cup, referred to above, was also eliminated since it would have resulted in a higher thermal resistance, and since it was believed that the solid slug type of construction of Figure 5-1 offers better protection for the glass seal. Having decided on a design of the general shape of Figure 5-1, some consideration was then given to other problems inherent in microminiature devices.

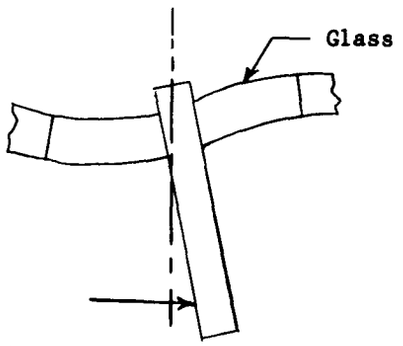


Figure 5-4

These additional considerations included the metal eyelet tooling (coining tool) and glass-to-metal seal tooling. It was also necessary to design special semiconductor processing tooling at this point; however, this is discussed below in connection with the process. In order to minimize height some speculation had to be undertaken on the minimum workable weld flange thickness. Also, to minimize height tolerance limits, the glass sealing operation had to be determined and held to a minimum. This was primarily to do with the location of the top of the feed-through post with respect to the top of the header surface. Grinding these posts flush with the header surface was considered as an alternative but later proved to lead to glass cracks. Also it was realized in the course of the development that it would be necessary to stretch the leads slightly upward, from the device, to avoid shorting in the centrifuge. Other inherent problems are mentioned in the following discussion. During the course of the development a variety of header thicknesses were tried in order to establish the minimum acceptable length of seal. Practically all of the geometrical parameters of the design were modified as the development proceeded.

3.2 FABRICATION PROCEDURES AND EQUIPMENT

3.2.1 and 3.2.2 DESCRIPTION OF PROCESS AND EQUIPMENT

The design and experimental work on the package was done jointly with two outside vendors of glass-to-metal seals. These were ITT Farnsworth of Palo Alto, California, and Zell Products of Norwalk, Connecticut. The development of this header was, of course, the principal aim of the task. It was also necessary to modify device packaging procedures to some extent. The devices for this task were supplied from Rheem's existing production of 2N697 dice. Since a TO-18 production line already existed it was possible to carry out all of the assembly operations on existing equipment with the exception of lead bonding. It was understood that Rheem would be using proprietary and existing equipment and processes for most of this task with the exception, of course, of the actual header development. The only change over existing procedures common to conventional TO-5 and TO-18 packaged units at Rheem was in the lead bonding area. Here, to conserve height, it was considered necessary to modify our standard wedge bonding procedure to attach the internal lead to the post as well as to the device. Internal lead bonding is discussed at some length in a later section of this report. Other changes from our process involved slight modifications of parts handling procedures and weld cycles at final sealing. Figure 5-5 shows the Kullicke and Soffa Model 401 lead bonder that was used. Figure 5-6 is a photograph of the final seal and bake-out unit which is also fairly standard.

3.2.3 EVALUATION OF PROCESS AND EQUIPMENT

Initial units were made on Kullicke and Soffa lead bonders with only a minor change in the Rheem TO-18 tooling. The change was to deepen the recess for the header flange in order to allow the thinner headers to protrude through the top of the heater block. This particular machine was not designed for production although many companies use it for this purpose. Since the lead welding was also carried out in this machine, immediately after lead bonding, production rates were comparable to those on the Rheem

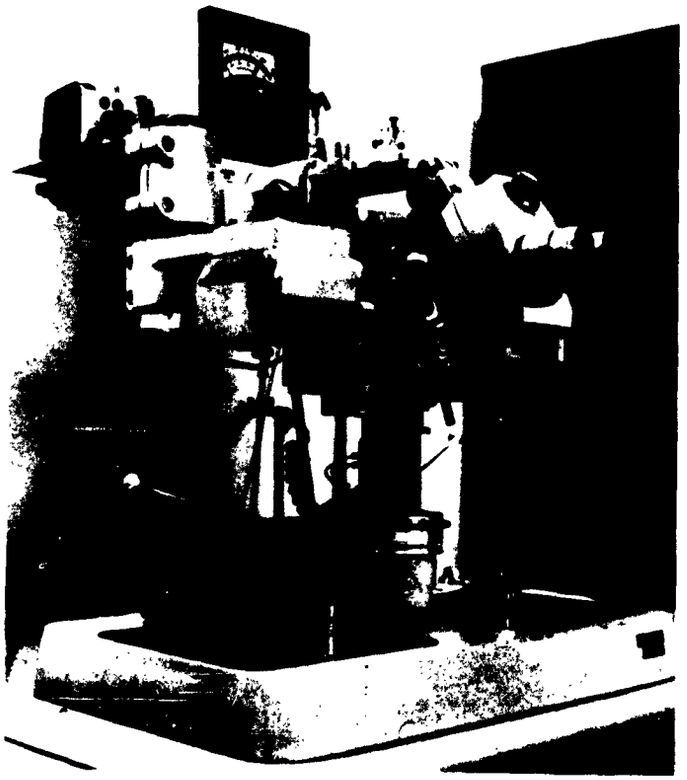


Figure 5-5. Kullicke and Soffa Lead Bonder

TO-5 production lines. This operation could be converted to a semi-automatic process by providing a rotating or sliding multiheader heater assembly. The final sealer was operated with no changes to the electrode design as compared to standard TO-18 operation; however, it was necessary to be much more critical about electrode alignment due to the thinner flange of the small units. During the early phases of this development an effort was made to use a header of 35 mil thickness and during this time a great many adjustments of dice-attach thermal-cycles and thermal and pressure cycles of the final seal were accomplished. It was later decided that this seal length would be unduly costly in high production from the standpoint of the glass-to-metal seal operation, especially in view of the reliability requirements. Hence, the header thickness was changed to 43 mils, which made all operations less critical. It was then found possible to handle these parts similarly to standard TO-5's or TO-18's.

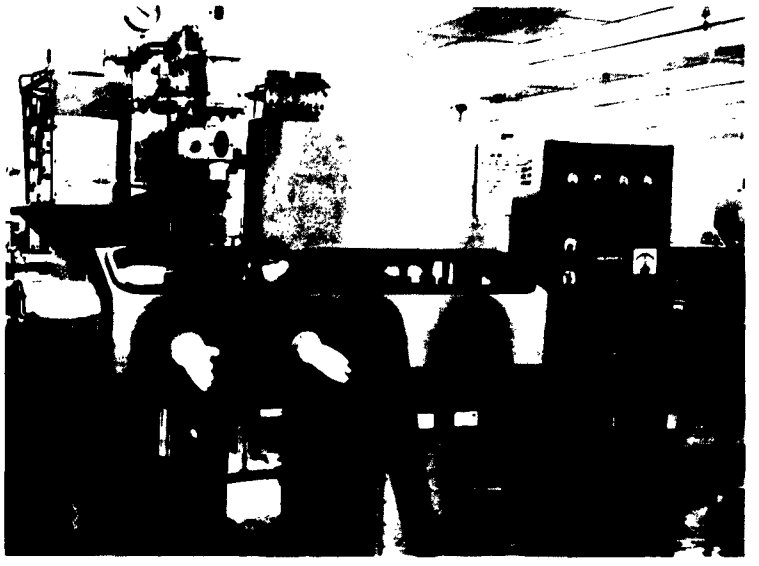


Figure 5-6. Final Seal and Bake-Out Unit

3.3 TEST PERFORMANCE AND DATA

3.3.1 DESCRIPTION AND PURPOSE OF TESTS

3.3.2 ANALYSIS OF PERFORMANCE DATA

3.3.3 TEST PROCEDURES

The requirements of the Electrical Performance (Group A) Tests, as given in the applicable RCA final specification, are exhibited in Table 5-1. All final 2N697 microelement transistors shipped to RCA under this task (18-5) successfully met these requirements. A photograph of this device both unmounted and mounted on a ceramic wafer, adjacent to a pencil point is included as Figure 5-10.

A group of 204 of these units were subjected to a Storage Life (Group C) Test at 200°C for 1000 hours. All of the transistors were within specified limits with regard to the parameters I_{CBO}, h_{FE}, and $V_{CE(SAT)}$ when measured at the completion of the test. An analysis of the Group C Test results is presented in Table 5-2 and in the parameter distribution graphs of Figures 5-7, 5-8, and 5-9.

TABLE 5-1
ELECTRICAL MEASUREMENTS (GROUP A) ACCEPTANCE TESTS FOR 2N697, TYPE B-4 TRANSISTOR

A-8978122, Rev. C
19 March 1962

Test	Measurements Acceptance Tests				
	Conditions	Sym.	Min.	Max.	Unit
Group A Collector cut-off current	V_{CB} = 30V I_E = 0	I_{CBO}	-	1	μAdc
Collector emitter voltage	I_{CER} = 100ma R_{BE} = 10 ohms PW ≤ 167μsec Duty Cycle = 1%	LV_{CER}	40	-	vdc
Emitter cut-off current	V_{EB} = 5V	I_{EBO}	-	.100	μAdc
Collector-emitter saturation voltage at 125°C PW = 300 μsec Duty Cycle ≤ 2.0%	I_C = 250ma I_B = 15ma	$V_{CE(sat)}$	-	4.2	vdc
Base emitter saturation voltage PW = 300 μsec Duty Cycle ≤ 2.0%	I_C = 250ma I_B = 15ma	$V_{BE(sat)}$	-	1.3	vdc
Small signal current gain at f = 20 mc	I_C = 50 ma V_{CE} = 10V	h_{fe}	2.5	-	-
DC Pulse Current gain at -30°C	I_C = 250 V_{CE} = 4V PW = 8μsec Duty Cycle = 20%	h_{FE}	19	-	-

TABLE 5-1 (Continued)

ELECTRICAL MEASUREMENTS (GROUP A) ACCEPTANCE TESTS FOR 2N697, TYPE B-4 TRANSISTOR

A-8978122, Rev. C
19 March 1962

Test	Measurements Acceptance Tests				
	Conditions	Sym.	Min.	Max.	Unit
DC Pulse Current Gain at -55°C	I_C = 250ma V_{CE} = 4V PW = 8μsec Duty Cycle = 20%	h_{FE}	15	-	-
Switching time (see test circuit)	I_C = 250ma V_{CC} = 10.75V IB_1 = IB_2 = 15ma PW = 8μsec Duty Cycle = 20%	td + tr ts + tf	- -	250 600	Mμsec Mμsec
Output capacitance	I_E = 0 V_{CB} = 10V	C_{OB}	-	35	uufd
Collector cut-off current at 125°C	V_{CB} = 30V I_E = 0 T_A = 125°C	I_{CBO}	-	100	uAdc
Thermal resistance	T_J = 200°C	C_{J-C}	-	75	°C/W

TABLE 5-2
FAILURE RATE AND ANALYSIS (GROUP C) TESTS

FAILURE RATE

ENVIRONMENT	DEGRADATION		INOPERABLE	
	MTBF	FRACTION DEF.	MTBF	FRACTION DEF.
200°C Storage Life 1000 hrs	223,000 at 60% confidence	.0045 per 1000 hrs	223,000 at 60% confidence	.0045 per 1000 hrs

TYPE TESTED
2N697, B-4
SPECIFICATION
A-8978122 Rev. C
DATE ISSUED (Spec)
19 March 1962

FAILURE ANALYSIS

SAMPLE SIZE	TOTAL HOURS	FAILURES	250 HOUR FAILURES	500 HOUR FAILURES	1000 HOUR FAILURES
204	204,000	$I_{CBO} = 0$		0	0
		$h_{FE} = 0$		0	0
		$V_{CE(sat)} = 0$		0	0

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS TA = 25°C	INITIAL LIMITS		END OF LIFE LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	$V_{CB} = 30V$ $I_E = 0$		1.0 μA		1.2 μA		1.2 μA
h_{FE}	$I_C = 250ma$ $V_{CE} = 4V$ PW = 8 μsec Duty cycle = 20%	19.		17.5		17.5	
$V_{CE(sat)}$	$I_C = 250ma$ $I_B = 15ma$ PW = 300 μsec TA = 125°C Duty cycle ≤ 2.0%		4.2Vdc		4.4Vdc		4.4Vdc

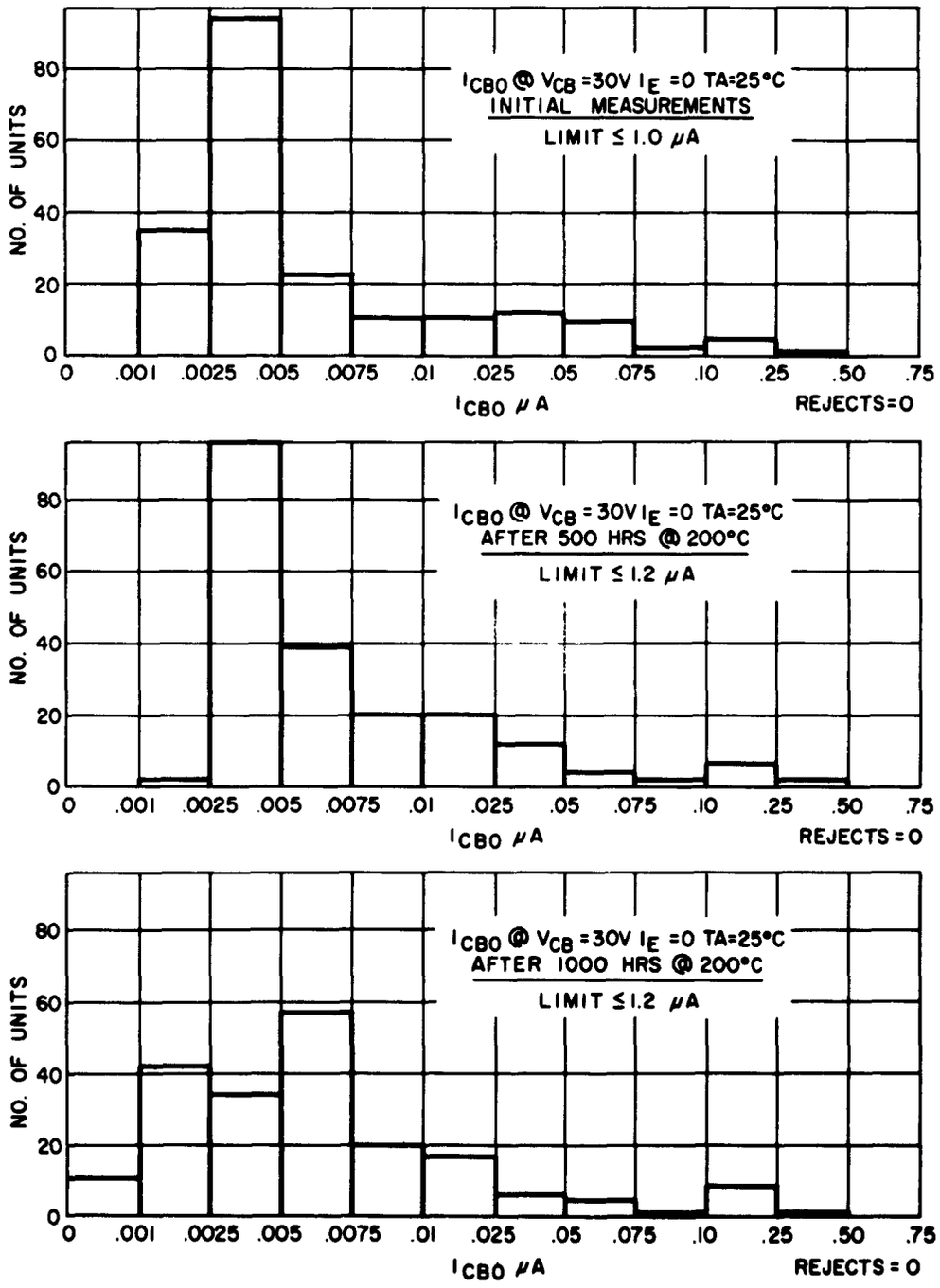


Figure 5-7. Units vs. I_{CBO} for 204 Rheem 2N697 Transistors

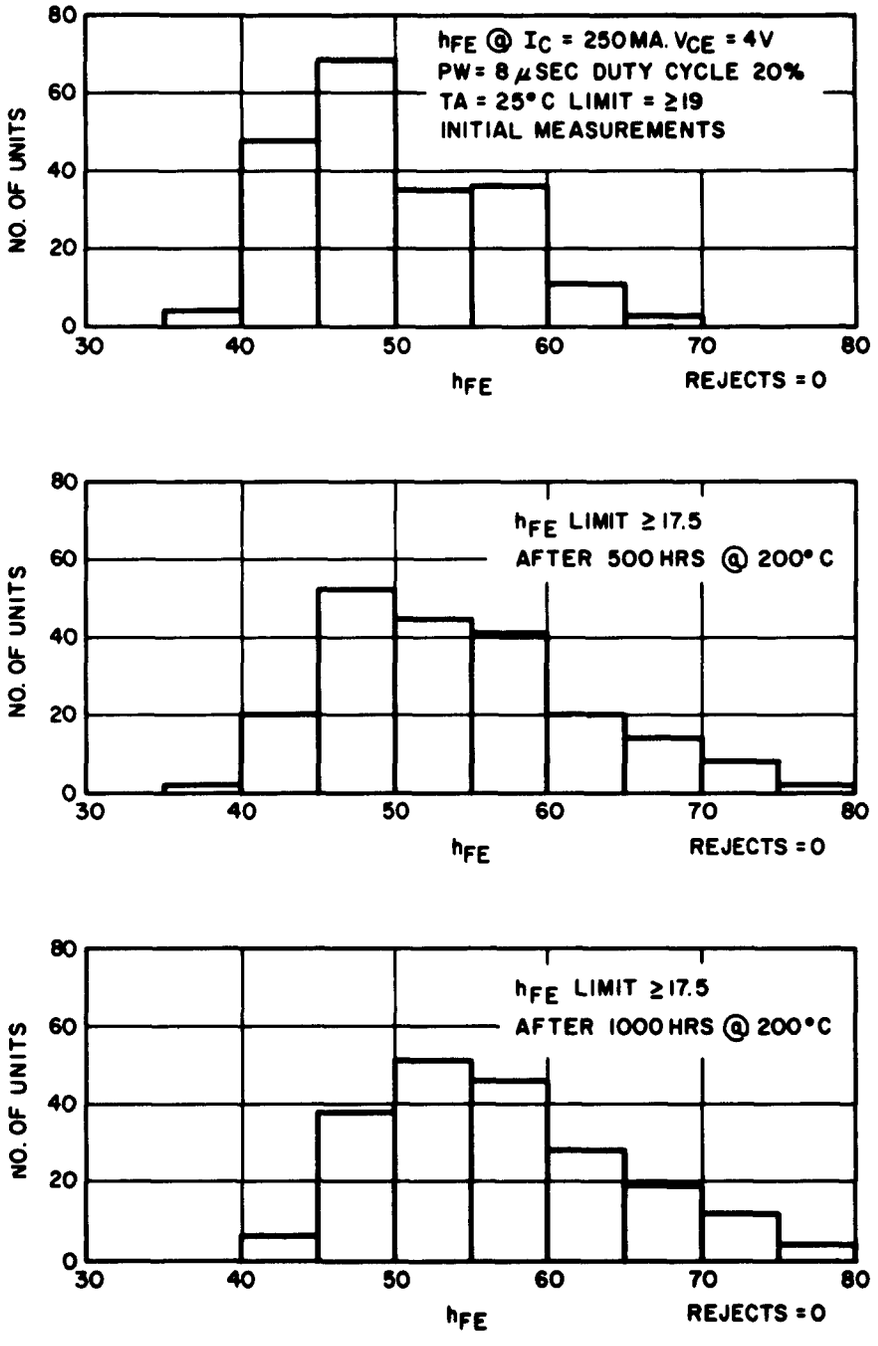


Figure 5-8. Units vs. h_{FE} for 204 Rheem 2N697 Transistors

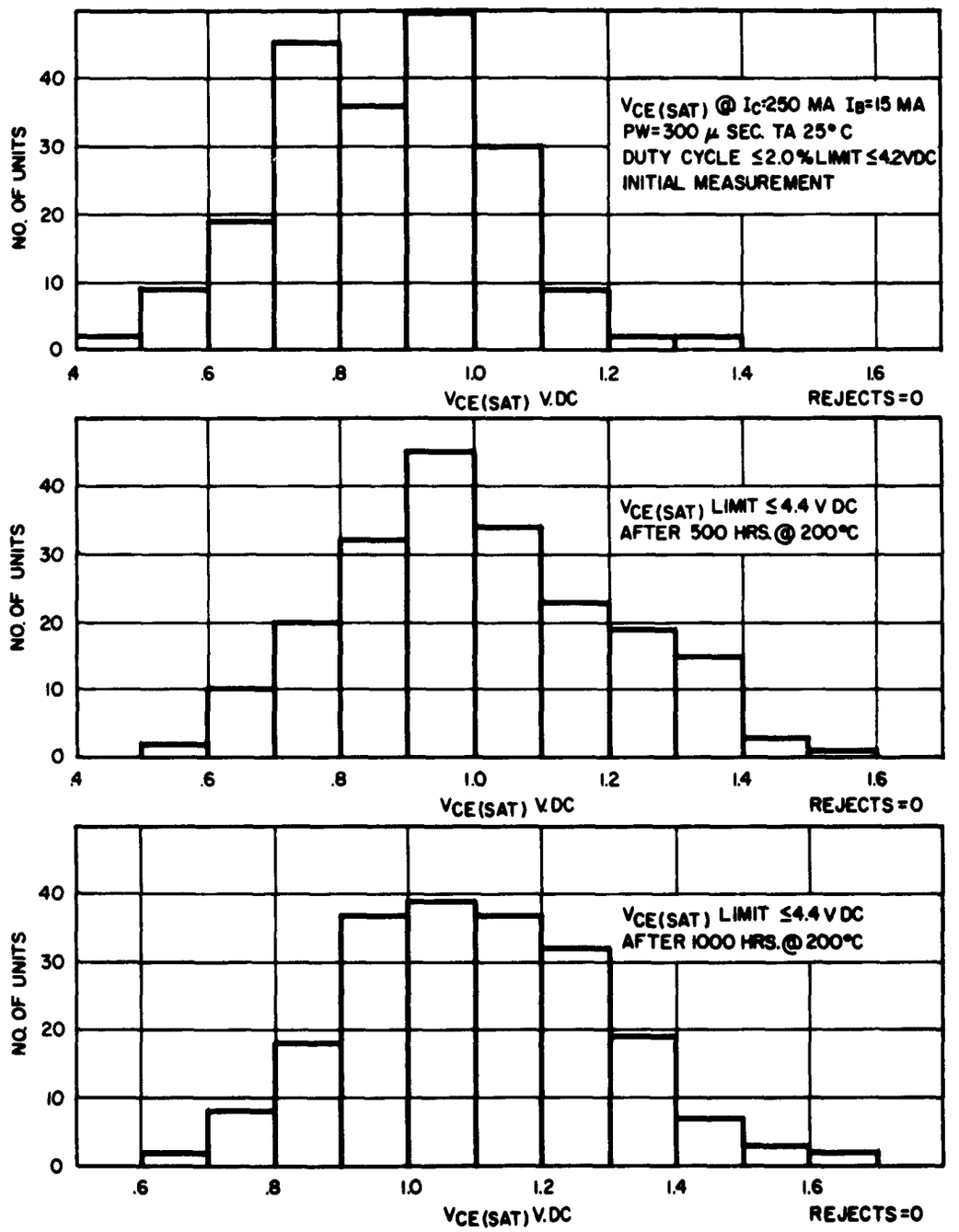


Figure 5-9. Units vs. $V_{CE(SAT)}$ for 204 Rheem 2N697 Transistors

TABLE 5-3
ANALYSIS OF ENVIRONMENTAL (GROUP B) TESTS

SUB-GROUP	TEST AND SPECIFICATION
I	a. Thermal Shock - 107 of MIL STD 202A Cond. A b. Moisture Resistance - 106A of MIL STD 202A 10 cycles
II	a. Centrifuge 40.4 of MIL-S-19500B (20,000 g's) b. Vibration 204 of MIL STD 202A Cond. C (non-spec)
III	a. Shock conforms with 202A of MIL STD 202A 500 g

TYPE TESTED
2N1132 B5
SPECIFICATION
A-8978121 Rev. C

SUB-GROUP	ENVIRONMENTAL CONDITIONS
I	a. 5 cycles at -55°C, 30 min.; 25°C, 10 min.; 85°C, 30 min.; 25°C, 10 min. b. Ten 24 hr. cycles variable temp. (25 to 65°C) relative humidity (90-95%)
II	a. 4 Orientations, one minute duration at 20,000 g's b. 2 hrs. in each of 3 orientations .06" max. 10-55-10 cps in 1.0 min. and 55 to 2000 cps in 35 ±5 minutes in 3 orientations.
III	a. 5 blows at 500 g minimum 1.0 milliseconds duration in each of four orientations X_1, X_2, Y_1, Y_2 (Total 20 blows)

FAILURE ANALYSIS

SAMPLE SIZE	SUB-GROUP	FAILURES	CLASSIFICATION OF FAILURES
10	I	0	
6	II	0	
6	III	0	

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS	INITIAL LIMITS		POST TEST LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	V_{CB} = -30V I_E = 0	-	-1.2	-	-1.2	-	-1.2
h_{FE}	V_{CE} = -4V I_C = 150 ma PW = 8μsec Duty Cycle 20%	15 (-55°C)	-	25	-	25	-
$V_{CE(sat)}$	I_C = 150 ma I_B = 8.5 ma T_A = 125°C	-	4.2	-	4.4	-	4.4

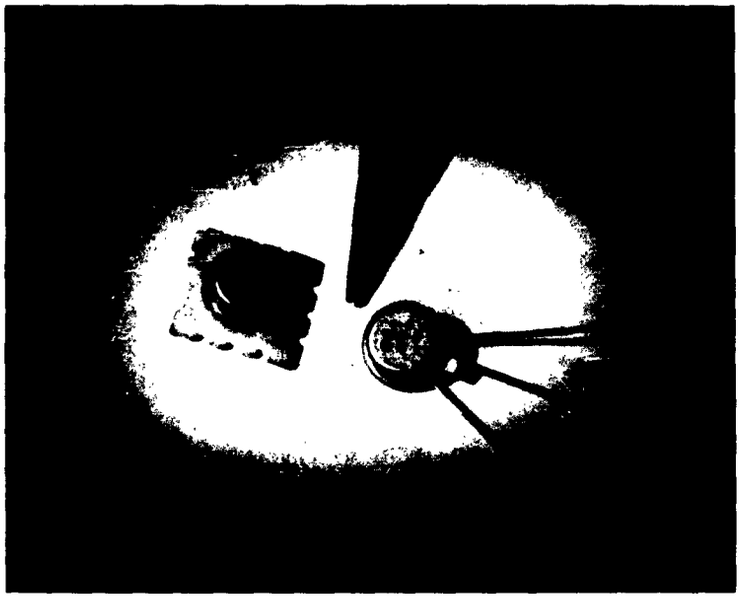


Figure 5-10. Rheem 2N697 Transistor of Task 18-5 (Magnification 5X) Adjacent to a Pencil Point

Twenty-two units selected at random from the lot, were subjected to Subgroups I, II, and III of the Environmental (Group B) Tests. All requirements of this test were successfully met by the transistors tested. An analysis of these tests is given in Table 5-3.

3.3.4 HISTORY OF HEADER DEVELOPMENT

A considerable effort was extended at Rheem and at the glass-to-metal seal vendors' plants during the earlier phases of the task, in attempting to establish the minimum seal length possible in mass production for reliable parts. Initially, seals from .015" to .045" were made in the laboratory at Rheem and at ITT Farnsworth. Glass cracking and leaks led to a decision, early in the development, to consider nothing under a .035" seal length (header height). After more than one hundred thousand units had been manufactured and tested it was the belief of Zell Products that the .035" header could be produced reliably. However, in view of the reliability requirements of the program it was jointly decided by representatives of RCA, The Signal Corps, Zell Products and Rheem Semiconductor that a .045" header would remove all doubt about the seal integrity. Subsequent tests of .045" headers indicated that units with this header thickness could be processed with no special precautions as compared to the standard TO-5 or TO-18 packages.

Long term, 200°C, storage tests at RCA produced some opens which were due to bond failures. Approximately 400 units were returned to Rheem for analysis. In September,

1961, Rheem started a program to improve the bond strength. The following section summarizes the results and gives the data and conclusion of this program:

Rheem Report on

Evaluation of New Bonding Technique

Summary

Data is attached indicating the superiority of the new wedge bonding technique over the old. Both new and old bonds were evaluated by various means of stress. A single new bond failure occurred. A total of 1534 units, both with new and with old bonds, were examined. These were divided into several groups. The stress levels for each group and details of failures are outlined below.

Test Results

In the following discussion, several groups of microblocs are considered. These are as follows:

I - 442 units returned from RCA. These are .035 headers, 3 stripe geometry, old bonding technique.

II - 200 units from class stores. These are .045 headers, triangular geometry, old bonding technique.

III - 436 units of new production. These are .045 headers, triangular geometry, 201 old bond and 235 new bonds manufactured from the same material.

IV - 416 units, same as III, 208 each new and old bonds.

V - 40 units, .045 headers, 3 stripe geometry. Planned sequence of bonds such that each unit has 4 new and 4 old bonds.

Group I

Preliminary data on this group was presented to RCA and the Signal Corps on October 10, 1961. These units were divided into two samples, subjected to a centrifuge test twice, examined before and after each such test and placed in 300°C aging test for 1000 hours. The centrifugal stress on Sample A was 20,000 g followed by 30,000 g. Seven failures were observed after first centrifuge test and no failures after second centrifuge. The centrifugal stress on Sample B was 30,000 g followed by 20,000 g. Ten failures were observed after first centrifuge and no failures after second centrifuge test. One failure was observed in each sample after 1000 hours aging. Seven failures were observed after 20,000 g centrifuge at the end of the 1000 hour aging.

Group II

These 200 units were a control on Group I. They were centrifuge tested at 20,000 g and 30,000 g, and then placed on 300°C aging test. One failure was observed at 500 hours and 3 failures at 1000 hours.

Group III

These 436 units (201 old and 235 new bonds) were divided into groups to be aged at various temperatures. Results are as follows:

Temp.	Wedge	# Units	Opens @250 hrs.	Opens @500 hrs.
300	New	58	0	0
300	Old	50	4	3
200	New	58	0	0
200	Old	50	0	0
125	New	119	0	0
125	Old	101	0	0

Note that all opens occurred at 300°C on old wedge bonds.

Group IV

These 416 units were subjected to the same stress as Group III. No failures have been observed up to 500 hours.

Group V

These 40 units were specially manufactured. Each unit had four old and four new bonds (posts and dies). These bonds were made in a prepared sequence and location. The units were then sealed and subjected to a series of stresses. Results as follows:

Stress	Failures: Old Bond	New Bond
1) 20,000 g centrifuge test	2	0
2) 30,000 g centrifuge test	1	0
3) @ 100 hours @300°C	0	0
4) 20,000 g centrifuge test	0	0
5) 30,000 g centrifuge test	0	0
6) @ 250 hours @300°C	2	1
7) 20,000 g	5	0
8) 30,000 g	0	0
9) @ 500 hours @300°C	2	0
10) 20,000 g	3	0
11) @ 750 hours @300°C	0	0
12) 20,000 g	1	0
13) @ 1000 hours @300°C	0	0
14) 20,000 g	1	0

Note the continuing failures of old bonds as compared to the single new bond failure.

Conclusions from the bond strength program

The test results obtained from five groups permit the following conclusions:

1. Groups I and II indicate that centrifuge and high temperature aging tests alone apply insufficient stress to sort out unreliable units.

2. Group III indicates that approximately 300°C is required to cause failures in a reasonable length of time (less than 1000 hours). This is the maximum storage temperature rating for our products.

3. Group V confirms the results of Groups I and II and, more importantly indicates the superiority of the new wedge bonding technique.

Accordingly, all microbloc production was converted to the new wedge bonding technique. Tests were contained on all five groups until each had 1000 hours of stress.

3.4 UNIT SPECIFICATIONS

The specifications in effect during this project, per paragraph 2.1, were:

RCA dwg. A-8978123 Hermetic Package for Micro Transistor

RCA dwg. A-8972091 Gen'l Specification for Micro Transistor

RCA dwg. A-8978122 Type B-4 Transistor

3.5 PRODUCT EVALUATION

Since the final TO-46 package design uses the TO-18 diameter and lead circle it is compatible with existing device packaging equipment in the industry. The use of a Kovar-glass seal and resistance welded closure has long been considered the most reliable closure for electron devices. This development has resulted in a package of the smallest possible height commensurate with the reliability requirements and the present state-of-the-art. The improvements in lead bonding, made during this program, are a substantial contribution and a necessity to the art of packaging devices for space restricted applications.

3.6 DELIVERY

2N697 Delivery Schedule

Qty.	Contract Date	Qty.	Actual Date
50	12-1-60	50	8-25-60
100	1-1-61		
50	2-1-61	150	8-31-60
150	2-1-61		
50	4-1-61		
100	7-1-61		
200	8-1-61	500	10-26-60
Total 700		700	

NOTE: Replacement shipment of 200 - 2N697 units was made on December 29, 1961.

4. CONCLUSIONS AND RECOMMENDATIONS

As a result of the work herein described it has been concluded (1) that .043" is a nominal seal length for headers of this type for the present state of the art of glass-to-metal sealing and semiconductor processing art; (2) that .065" is a nominal height for axial lead packages for collector mounted devices of these types; and (3) that the TO-46 package is fully as reliable as the conventional TO-18 or TO-5 configurations.

SECTION VI

FORMAL ENGINEERING REPORT
ON
TRANSISTOR PACKAGE
TASK 18-6
MICRO-MODULE PROGRAM EXTENSION I

PO GX1-946252-5771

HERMETIC PACIFIC
ROSEMEAD, CALIFORNIA

PO GX1-946252-5770

ZELL PRODUCTS
NORWALK, CONNECTICUT

PO GX1-946252-5769

ISOTRONICS, INC.
LODI, NEW JERSEY

PO GX1-946252-2560

VERITRON WEST
NORTH HOLLYWOOD, CALIFORNIA

November 15, 1962

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1. PURPOSE OF TASK 18-6

Early in the Micro-Module Program, microelement transistors were extremely costly due to marginal packaging techniques. The transistor element was mounted in a recessed ceramic wafer and sealed by soldering a metal disc over the recess. In addition to low production yields, only fair reliability was obtained. Two major purposes of Task 18-6 were to develop transistor packages for greater reliability and to lower transistor costs.

2. ABSTRACT

In order to utilize a maximum of state of the art techniques, four vendors were selected to develop five different package designs. All of the companies selected for the task were actively engaged in production of conventional transistor packages.

The greatest success, and by far the outstanding contribution of this task, was the development of the TO-46 transistor package. This package is one of the smallest, most reliable packages used in the transistor industry today.

In all cases, the greatest problem encountered in this task was the development of a glass to metal seal in a reduced physical size. Prior to this program, transistor package seals depended quite heavily on massive glass-to-metal joints. In addition to sealing problems, tolerances were tightened to compensate for smaller size. Transistor manufacturers are interested only in packages that are adaptable to tried and proven methods of manufacture. Therefore another prime consideration in package design was the ease of transistor manufacture.

As a result of this task, the Micro-Module Program was provided with a reliable and inexpensive transistor package. Initially contracts were placed for four different packaging concepts. After evaluating samples received from these contracts, the package which showed the greatest promise was selected as the primary package for the microelement transistor. The facts learned by other package designs provided valuable information toward achieving success in the TO-46 package.

3. NARRATIVE AND DATA

3.1 DESIGN CONSIDERATIONS

The Hermetic Pacific Corporation of Rosemead, California, was granted a contract to develop two transistor package designs. The first design (Figure 6-1) was directed at a package for use on micro-module wafers only. The benefit sought in this design was ease in mounting to the wafer. Figure 6-1 shows the stacked construction of this package. Part 1 is an .008" thick kovar disc which acts as the collector lead of the transistor and as the bottom seal. Parts 2 are glass rings which are fused to the kovar parts for sealing and lead insulating purposes. Part 3 is a ring of kovar metal

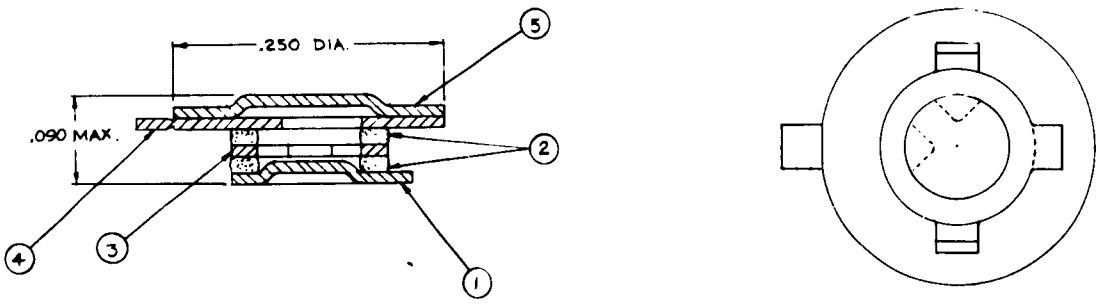
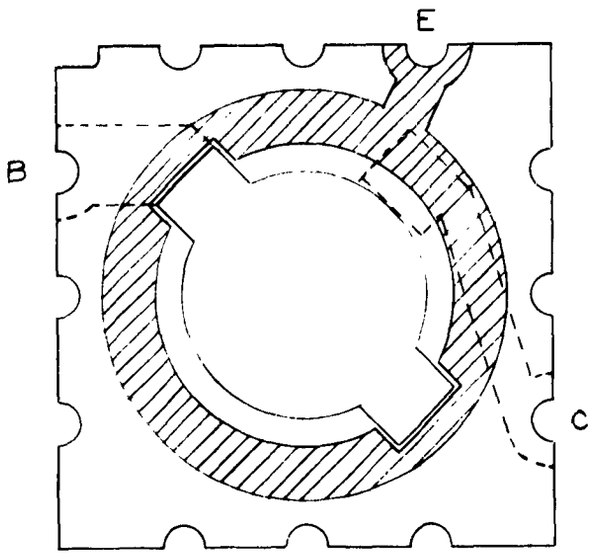


Figure 6-1. Stacked Package, Hermetic Pacific Corp.

which is the base lead of the transistor. Part 4, of kovar, is the emitter lead. Part 5, also of kovar, is used to seal the transistor assembly. Figure 6-2 shows the ceramic wafer designed for this package. The package is placed into the notched hole with the collector and base leads soldered to metalization on the far side, and the emitter disk soldered to a ring of metalization on the near side.

Figure 6-3 shows the original design of Hermetic Pacific's second package. After mounting the transistor element on the raised portion of the base, and making emitter and base connections, the package is sealed by welding on the cap. Figure 6-4 shows the design which replaced Hermetic Pacific's original designs in order to satisfy hermeticity requirements. This design is similar to the TO-46 package except that a single glass seal is employed instead of the conventional two seals.

Zell Products of Norwalk, Connecticut was given a contract to design and develop the package shown in Figure 6-5. This package was designed with radial leads to facilitate mounting on the wafer and to obtain a low height. Figure 6-6 shows this package mounted on a wafer. This design was abandoned because it did not lend itself to volume production at low cost.



NOTE : THICKNESS — .035

Figure 6-2. Wafer for Stacked Package

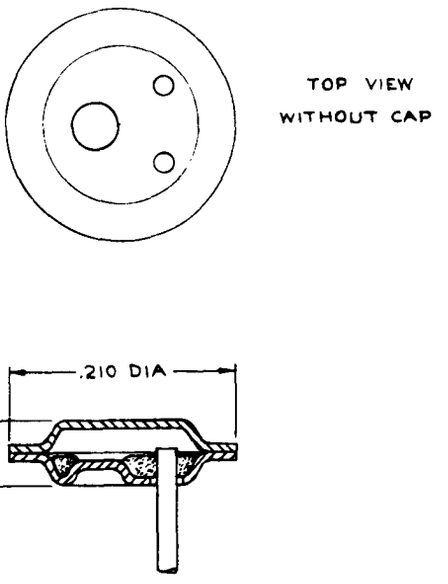
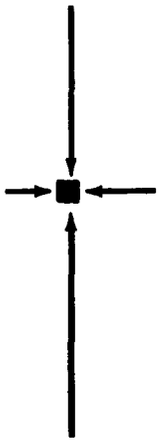


Figure 6-3. Design #2, Hermetic Pacific Corp.



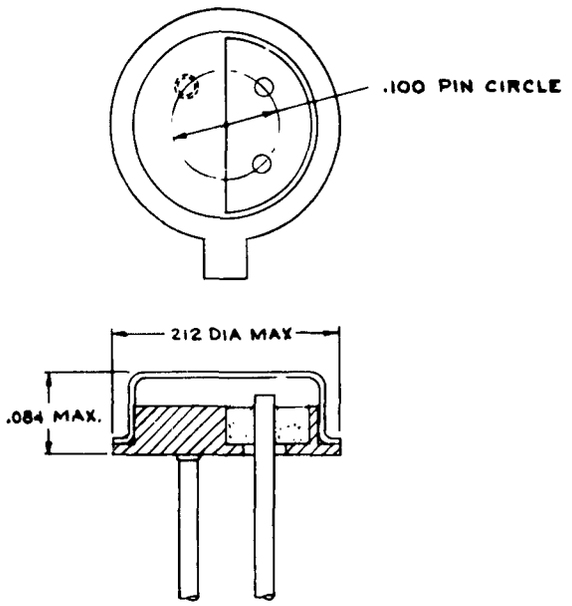


Figure 6-4. Modified TO-46, Hermetic Pacific Corp.

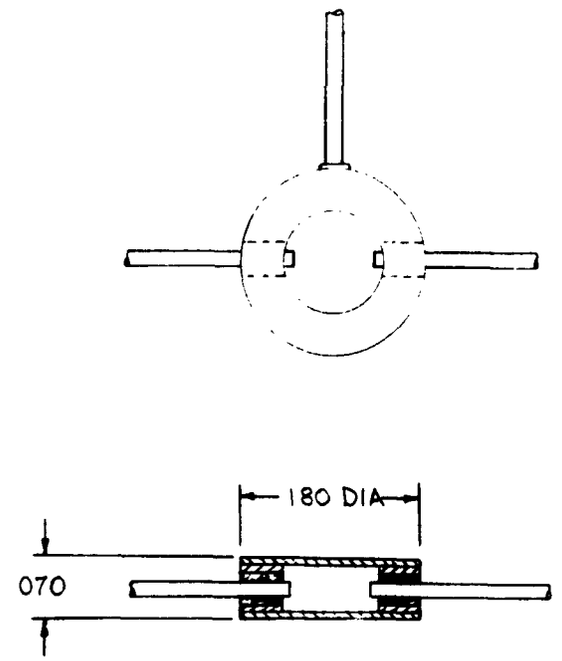


Figure 6-5. Radial Lead Package of Zell Products

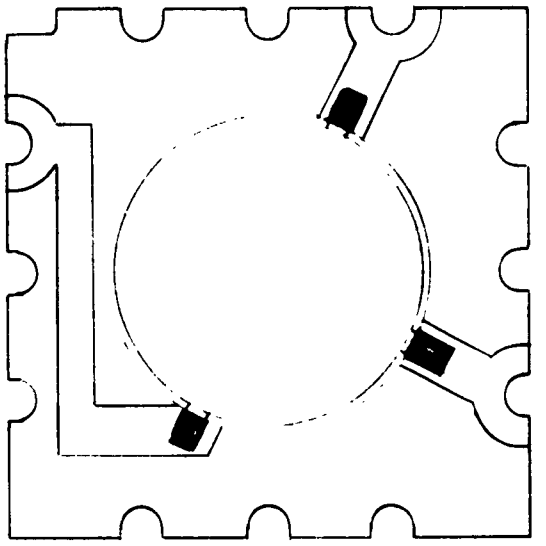


Figure 6-6. Mounted Radial Lead Package of Zell Products

Isotronics, Inc. of Lodi, New Jersey, was given a contract to design and develop the transistor package shown in Figure 6-7. This design is similar except for dimensions, to the TO-46 design. Of all designs submitted, this one provides the greatest area for mounting the transistor element.

Veritron West, Inc. of North Hollywood, California, contracted to develop the design shown in Figure 6-8 and in the photograph (magnification 5x) of Figure 6-9. This package was originally designed by Rheem Semiconductor Corporation and produced by Zell Products. In the course of developing microelement 2N697 and 2N699 transistors, Rheem had considerable difficulty in obtaining reliable hermetic packages from their original design. Veritron West claimed that the package could be sealed reliably if the header height was increased from .035 to .042 inches. As predicted, the increased height permitted a longer glass-to-metal seal which was found to provide a significantly higher yield of hermetic packages.

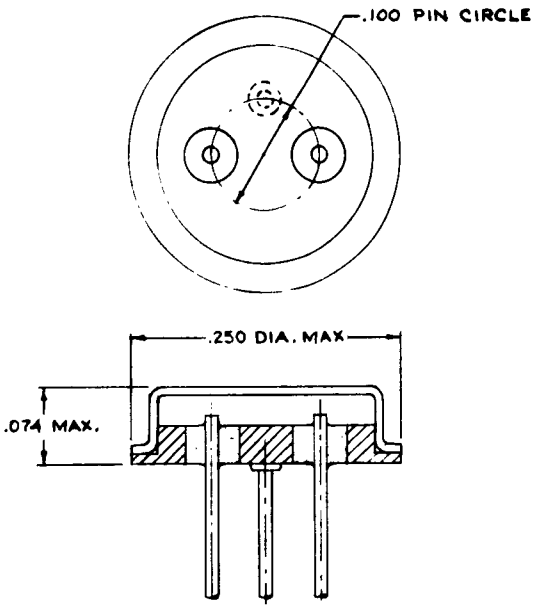


Figure 6-7. Isotronics Package

3.2 FABRICATION PROCEDURES AND EQUIPMENT

3.2.1 DESCRIPTION OF PROCESS

The following is a description of the fabrication of the TO-46 header in production. This process, with minor variations, is used for all packages developed in the task. A flow chart of this process is exhibited in Figure 6-10.

The collector lead is jig-oriented and butt-welded to the kovar body blank. This assembly is then placed in a 100 to 500 place carbon fixture. The two glass beads are shaker loaded, and the two leads are hand placed. When fully loaded, the carbon fixture is placed into a belt-fed furnace. The furnace contains an oxidizing atmosphere, and while the parts are heating to the melting temperature of the glass, the metal parts oxidize. When the parts are heated to 1750°F, the glass wets, or fuses to, the oxide coating of the kovar leads and body. After remaining in the furnace chamber for ten minutes, the fixture and headers enter an annealing chamber. The annealing cycle lasts for approximately 30 minutes, and cools the parts to 500°F. The headers are cooled to room temperature and inspected visually for defects. A sample quantity is tested for mechanical strength by lead bending and pull tests. The headers are pickled in inhibited HCl to remove the excess oxide. The next manufacturing step is to clip the emitter and base posts to approximately .020 and then grind the posts

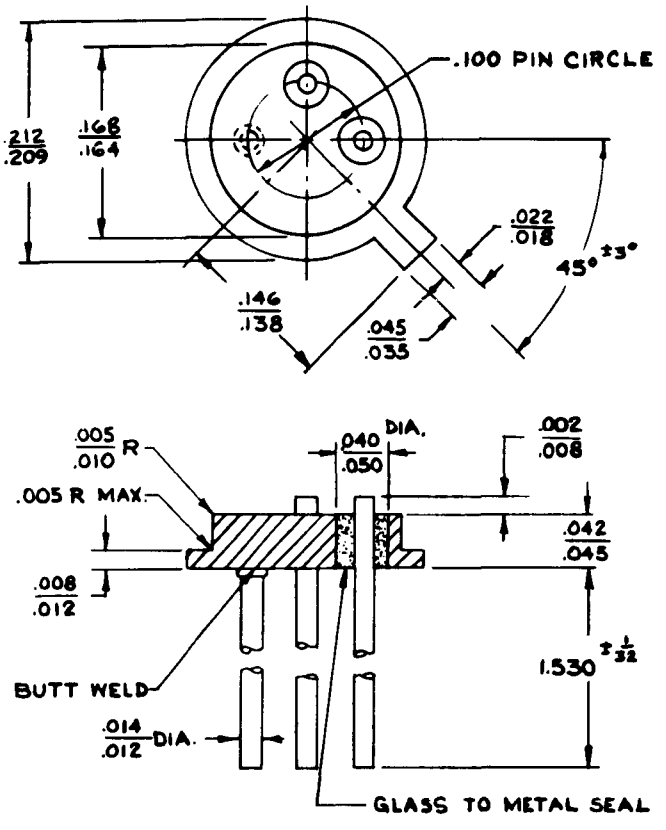


Figure 6-8. TO-46 Veritron West, Inc.

to the specified length. The headers are prepared for plating by a chemical "bright dip". The plating consists of an electrolytic deposit of gold .00006 inch thick. Each production run is sampled for quality control tests. The sample headers are inspected for plating, continuity of the glass seal, lead strength, and strength of seal.

3.2.2 EVALUATION OF PROCESS AND EQUIPMENT

In view of the low cost and high yield of the process described, there is little need for improvement. Machinery could probably be built to automate the entire process, but the capital required would not be justified by the savings. The only weak link in the process is the use of carbon fixtures. These carbon tools are costly to make, and require frequent replacement. At present, however, carbon is the only practical material to use due to its temperature stability and relatively low cost. A search for a material of better durability and equal or lower cost could be very worthwhile.

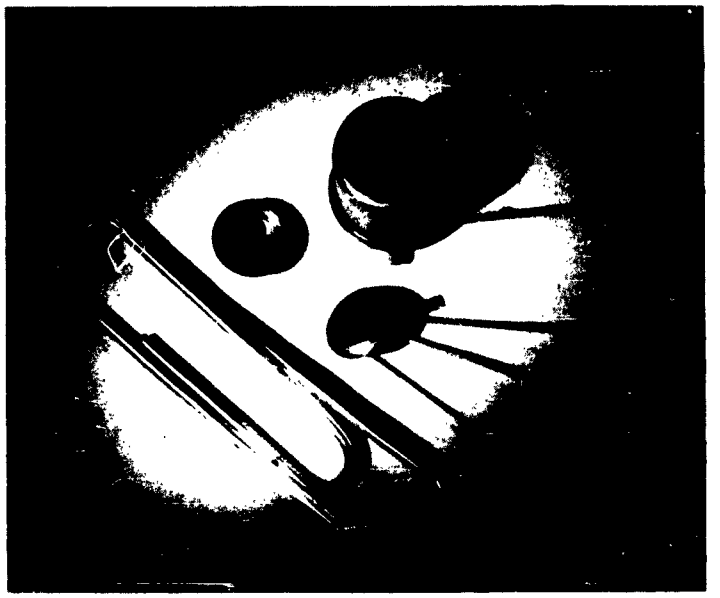


Figure 6-9. TO-46 Header and Cap of Task 18-6 (Magnification 5x) Adjacent to a 1 ¼ inch Paper Clip (Standard TO-5 Transistor also shown)

3.3 TEST PERFORMANCE AND DATA

3.3.1 DESCRIPTION OF TESTS

The following is a description of the test requirements as stated in the RCA purchase description for the transistor package.

Visual and Mechanical - The header and case shall be examined for conformance to specifications on materials, design and construction, plating and workmanship.

Temperature Cycling - Temperature cycling shall be conducted in accordance with MIL-STD-202A, method 102A, test condition C. This test is used as a preconditioning in conjunction with the pin seal and package seal tests. No measurements are required after the immersion test.

Pin Seal Test - The header shall be equipped with suitable gaskets and tested with an approved helium leak detector (sensitive to 6×10^{-9} standard cc per second).

Package Seal Test - Insofar as possible, the cap shall be assembled to the header by the use of standard assembly techniques. The package then will be drilled, equipped with suitable gaskets, and tested for leaks with an approved helium leak-detector.

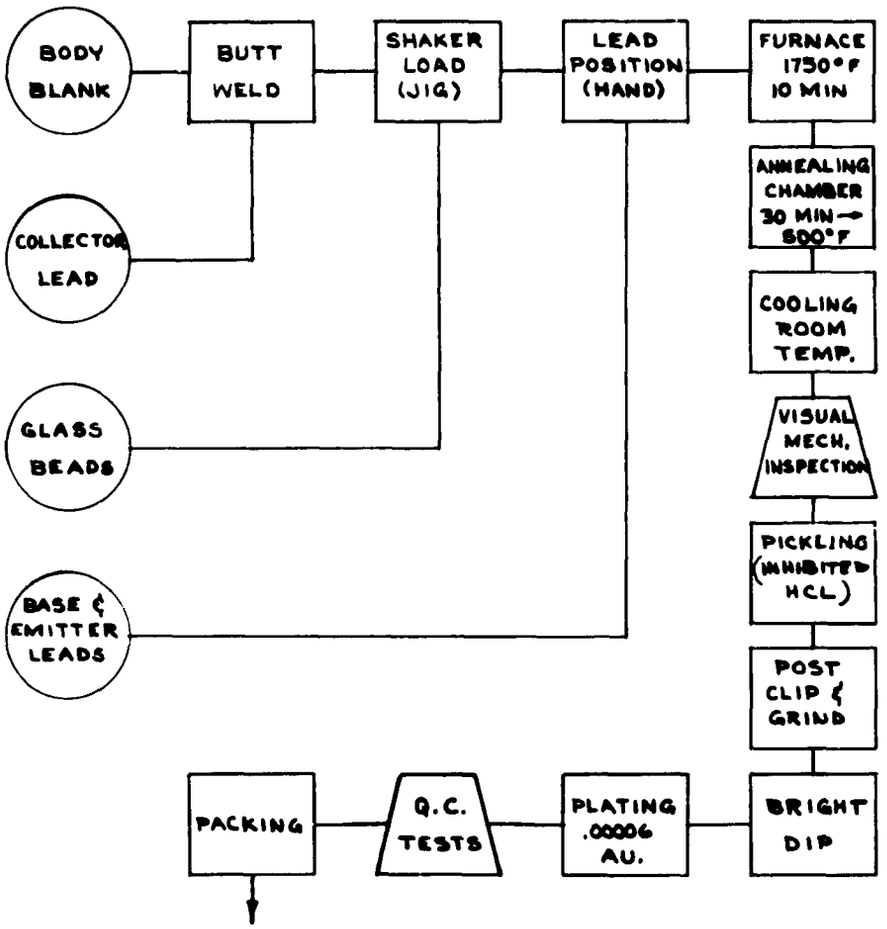


Figure 6-10. Flow Chart for TO-46 Package

3.3.2 and 3.3.3 ANALYSIS OF PERFORMANCE DATA AND TEST PROCEDURES

The original stacked design package of Hermetic Pacific (Figure 6-1) was not tested beyond the visual and mechanical test due to very poor mechanical strength. Under normal handling, the glass-to-metal bands fractured. The vendor could not obtain a suitable band within the allotted time and was therefore advised to abandon the design.

A sample quantity of the second Hermetic Pacific package design (Figure 6-3) (twenty-two sealed samples) was subjected to pre-conditioning tests and then to the package seal test. Thirteen of the twenty-two samples indicated a leak rate in excess of 6×10^{-9} cc/sec. Due to this high failure rate and the delivery time requirements, the vendor was advised to abandon the design.

After receiving samples of the design shown in Figure 6-7 from Isotronics, 43 unsealed and 61 samples were subjected to the pre-conditioning tests. Helium leak checks indicated no failures in either the pin seal or package seal tests.

Fifty-seven (57) sealed and fifty-one (51) unsealed samples of Zell Products radial lead package (Figure 6) were subjected to preconditioning tests. A helium leak check indicated 31 of 51 sealed units had excessive leak rates. The unsealed units were not adaptable to helium leak checks, and were therefore dye checked. The samples were placed on a level surface and were filled with dye (spot check penetrant #2, Magnaflux Corp.). At the end of one hour, twelve samples showed leaks at one or both glass seals; twelve leaked at the bottom cap, and twelve leaked at both the glass seals and bottom cap. In view of this high failure rate, the work on this package was terminated.

The TO-46 package from Veritron West Inc. (Figure 6-8) was subjected to preconditioning tests in addition to those described previously. Information obtained from transistor manufacturers indicated that the thermal shock encountered during application of the die was the major cause of glass-to-metal failures. The packaging group at RCA, Somerville designed a pre-conditioning test to simulate stresses encountered during transistor manufacture. The test was performed on the Veritron package as follows:

Fifty-four (54) unsealed packages were inspected visually for mechanical defects with no resulting rejects. The samples were then subjected to a helium check for pin seal and again no failures occurred. Twenty-five of these packages were preheated to 200°C ±25°C in ten to 15 seconds and then heated to 425°C +0/-5°C in 15 to 20 seconds. This thermal shock, which is similar to that encountered during the application of die, produced no failures when subjected to a helium leak check. These 25 samples along with the other packages not subjected to thermal shock, were sealed and subjected to a helium bomb at 40 psi for four hours. The fifty-four samples were then subjected to a helium leak check with a sensitivity of 1.4×10^{-11}cc/sec. The sealing process, which is identical to production transistor sealing, produced no failures.

Because of the success of this package design and the probability that it would enjoy widespread use, a sample quantity of 25 packages was subjected to the following test to determine how great a thermal shock they could withstand. The packages were preheated to 200° ±25°C in 10 to 15 seconds and then thermal shocked to the following temperatures within 15 to 20 seconds.

Shock Temp. °C	425	465	500	535	570	600
Failures among 25 packages (Helium leak detector)	0	0	0	0	0	3

The package developed by Hermetic Pacific as a variation of the TO-46 design (Figure 6-4) was tested in a manner similar to that for the Veritron package. Fifty-one (51) samples were inspected visually and then subjected to a helium leak check for a pin seal test. Two of the 51 samples indicated a leak rate in excess of 5×10^{-8} cc/hr. The remaining forty-nine (49) units were preheated to 200° ±25°C in 10 to 15 seconds and then heated to 425° +0/-5°C in 15 to 20 seconds. A helium leak check indicated that two more units leaked in excess of 5×10^{-8} cc/hr. The remaining units (47) were sealed and subjected to a helium bomb for four hours. At the end of the period the units were helium leak checked and no additional failures were encountered.

3.4 UNIT SPECIFICATIONS

The specification governing the design and quality of the packages developed in this program is RCA drawing A-8978123, dated 17 June 1960, and amended 30 September 1960. This document specifies samples required, materials, design and construction, plating, workmanship, and quality assurance. As explained earlier in this report, the pre-conditioning tests were altered for the TO-46 package from Veritron West and the modified TO-46 package from Hermetic Pacific.

3.5 PRODUCT EVALUATION

(Included in Paragraph 3.3.3)

3.6 DELIVERY

A quantity of 2100 each of Hermetic Pacific's two original package designs were scheduled for delivery to RCA in October of 1960. Due to extreme technical difficulties, samples of only the first stacked package (Figure 6-1) were received by October 1960. Samples of the second type (Figure 6-3) were not received until December 1960. As stated in the test results, both lots of samples failed to meet requirements and due to time and feasibility requirements these designs were abandoned.

The Hermetic Pacific contract was rewritten to cancel the original two designs and to substitute the third design (Figure 6-4) at a lower total cost. The contract then called for a quantity of 200 acceptable packages to be delivered by September 15, 1961. The vendor completed this task on August 23, 1961.

Zell Products contracted to deliver 2100 packages of the radial lead design (Figure 6-6) in October of 1960. Again, due to extreme technical difficulties, samples were not supplied for testing until March, 1961. The samples failed to meet requirements and due to the complexity of this design, and time factors, this design was abandoned. The contract to Zell Products was cancelled, and, due to the effort expended by Zell, a partial payment of the contract price was allowed.

Isotronics, Inc. was awarded a contract for delivery of 2100 packages (Figure 6-7) by March 15, 1961. The vendor supplied test samples in December of 1960 and, on the basis of satisfactory test results, was given permission to deliver final packages. Delivery of the final packages was completed on March 15, 1961.

Veritron West, Inc. contracted to deliver 1000 packages of the TO-46 (Figure 6-8) design by May 1, 1961. The vendor experienced minor difficulties in obtaining kovar blanks to his specifications, and consequently, was slightly late in making delivery to RCA. A shipment of 200 parts was received at RCA on May 14, 1961, and the balance of 800 units received on May 27, 1961.

4. CONCLUSIONS AND RECOMMENDATIONS

4.1 CONCLUSIONS

As previously stated, the purpose of this task was to obtain a reliable, inexpensive hermetic package for microelement transistors. This effort did, in fact, accomplish this purpose in the TO-46 package. This package is not only being used in micro-module applications, but has received manufacturers' approval for conventional purposes. During the development of the TO-46 package, a minimum header thickness of .042 inch for the glass-to-metal seal was found to be necessary for high reliability. A thinner header with less glass area making contact with the feed-through hole is considered marginal. The package designed and developed by Isotronics was also a technical success. The only reason for its lack of acceptance by the manufacturers was the availability of the smaller TO-46 package.

4.2 RECOMMENDATIONS

The manufacturers of microelement transistors have been supplied with a package of suitable size and construction. It is now up to these manufacturers to set up their own acceptance criteria or perhaps to adopt a universal incoming inspection procedure. If the manufacturers were to adopt such a procedure, the package vendors could achieve better uniformity and possibly reduce prices.

New ideas for package designs should be sought and encouraged. The Micro-Module Program would benefit greatly from the development of a package under .050 in height. Such a package, of course, would be required to provide the same reliability and ease of processing as present package designs and at a reasonable cost. The package vendors should be encouraged in efforts to reduce manufacturing cost. As previously mentioned a new material for more durable firing jigs would be beneficial to prices.

SECTION VII

FORMAL ENGINEERING REPORT
ON
CERAMIC WAFERS FOR THE
TRANSISTOR PACKAGE
TASK 18-7
MICRO-MODULE PROGRAM EXTENSION I

PO GX1-946264-0649-24-D30

MITRONICS
MURRAY HILL, NEW JERSEY

PO GX1-946256-3103-24-D30

CERAMICS FOR INDUSTRY
MINEOLA, NEW YORK

November 15, 1962

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1. PURPOSE OF TASK 18-7

The primary purpose of this task was to design and produce ceramic wafers for mounting the transistor packages developed in Task 18-6.

2. ABSTRACT

Two vendors were selected for the wafer task. Mitronics, Inc. of Murray Hill, New Jersey, was awarded a contract to furnish five different wafer designs with twenty-five samples each. In addition, this contract called for one-thousand each of two selected wafer designs chosen from the original five designs. Ceramics for Industry of Mineola, New York, was awarded a contract for the development and production of recessed wafers for Sylvania's 2N404 transistor (Task 18-9).

In Mitronics' original proposal, they submitted wafer designs for the proposed package designs of Task 18-6. It was decided, however, to release the wafer designs as the package samples became available. This precaution was very well taken as evidenced by the failure of some of the package designs.

In order to clarify wafer nomenclature, Figure 7-1 is presented to illustrate the wafer and its terminations. Figure 7-2 is presented to give the standard dimensions and tolerances of a wafer.

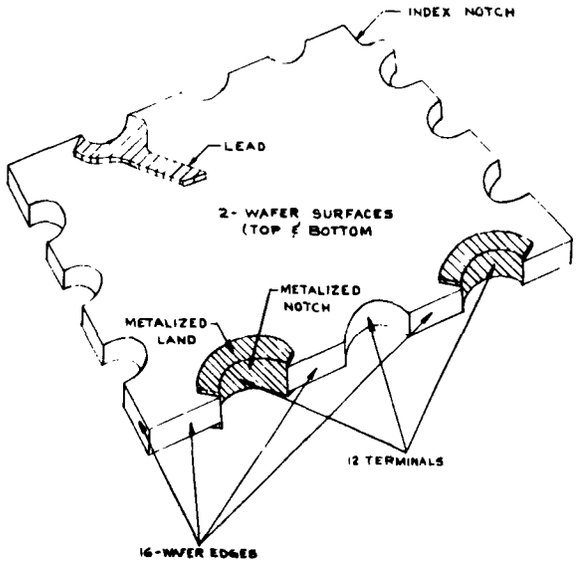


Figure 7-1. Wafer Nomenclature

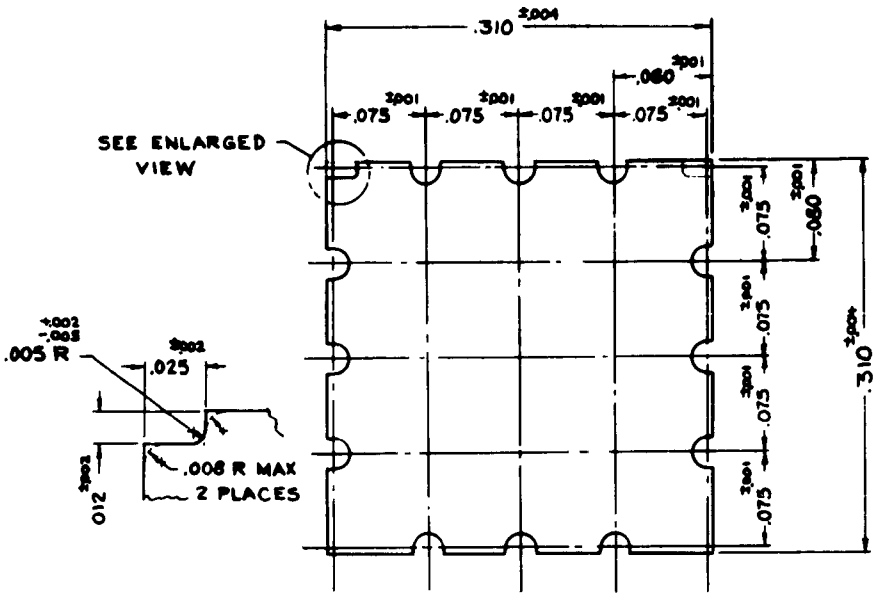


Figure 7-2. Standard Wafer Dimensions

3. NARRATIVE AND DATA

3.1 DESIGN CONSIDERATIONS

The first wafer design released for a prototype run is shown in Figure 7-3. This wafer was designed for mounting the transistor package used by Rheem Semiconductor on Tasks 18-2 and 18-5 (Sections II and V of this report). The diameter of the collector hole is larger to accommodate the butt welded collector lead. This wafer design was selected as one of the final design types due to the success of the Rheem package. After reliability improvements, by Veritron-West and Hermetic Pacific, this became known as the TO-46 package.

Figure 7-4 shows a design chosen for use with the Sylvania .250 diameter package. Mitronics was approached on making a recessed wafer for this package but had reservations on thin wall sections which would be required. The small bulges or projections on Figure 7-4 were designed to position the .250 package centrally on the wafer to prevent shorting to the central riser wire.

Ceramics for Industry was confident of obtaining good results with the wafer shown in Figure 7-5. The thin wall sections between the recessed hole and the center notches did not deter their confidence. It was felt that this design would offer maximum protection against shorting of the .250 package to the central riser wire. After further

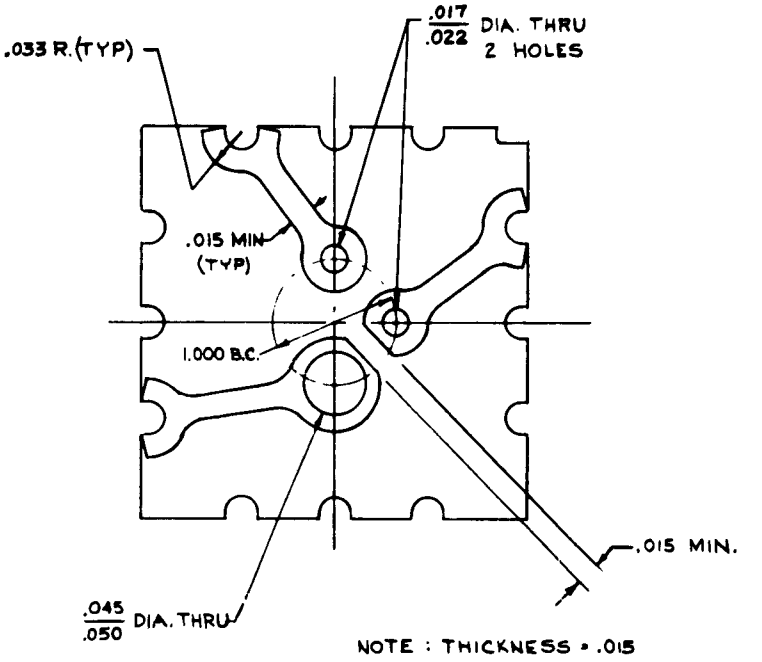


Figure 7-3. Design Number 1, Mitronics

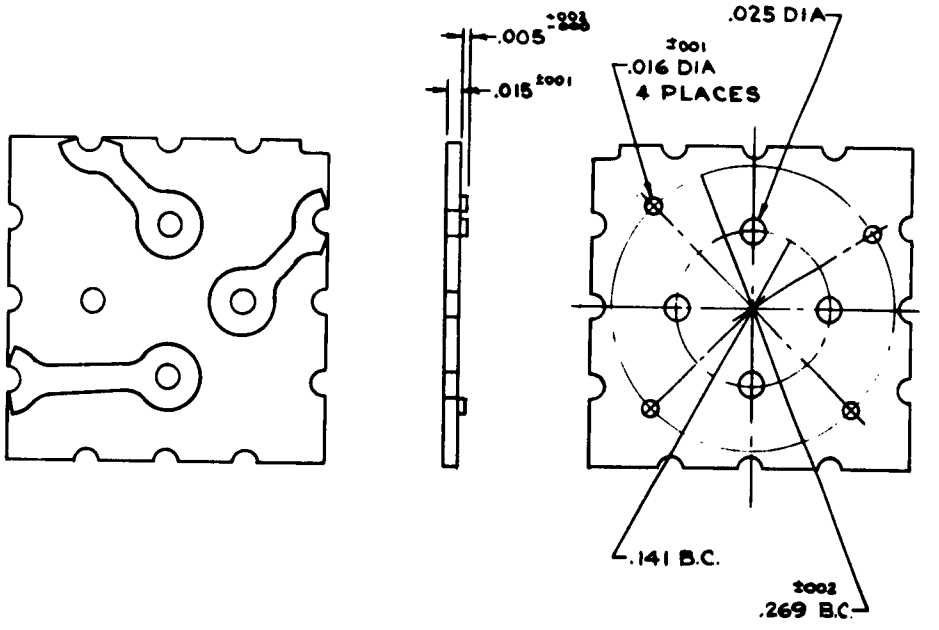


Figure 7-4. Design Number 3, Mitronics

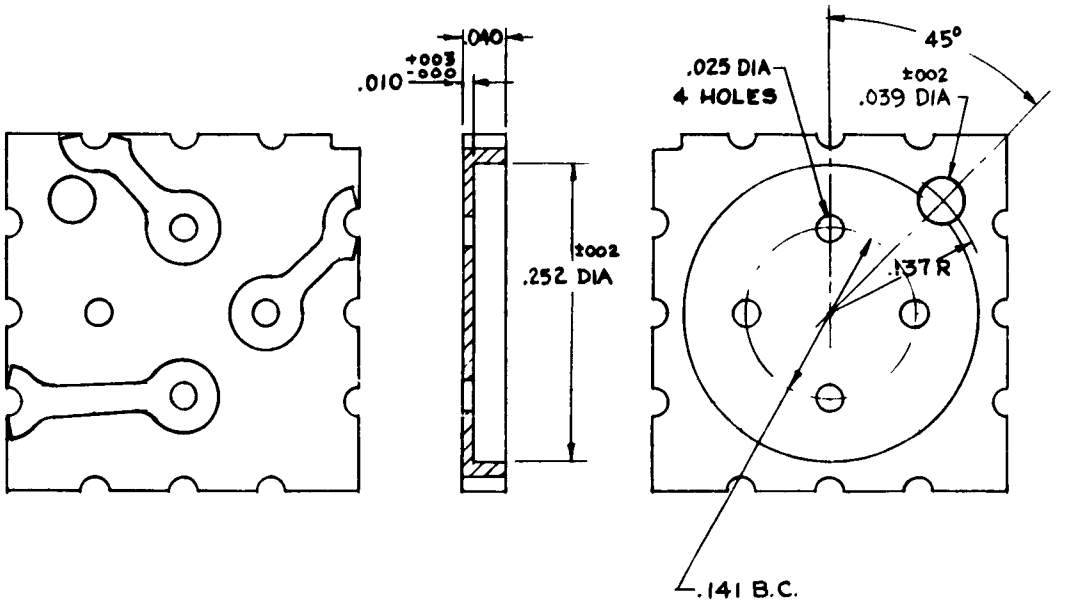


Figure 7-5. Recessed Wafer, Ceramics for Industry and Mitronics

consideration of the thin wall problem, Mitronics also agreed to make a sample quantity of this design as the third of its five designs.

Some concern was expressed by module reliability personnel over moisture becoming trapped under transistors during mounting. To combat this possibility, the wafer shown in Figure 7-6a was designed. The large central hole was designed to prevent moisture from becoming trapped beneath the transistor. Later, in a production order of this design, the metalization pattern was altered as shown in Figure 7-6b. This change was made for conformance to RCA Land and Lead Specification 492984.

A major reliability problem was encountered in diode mounting. Diodes are mounted to wafers by high temperature solder. The existing problem is "popped" joints during riser wire solder operations. The diodes are under various stresses when soldered to the wafers, and under riser wire soldering operations, enough heat reaches the overstressed joints to cause some of these to open. Welding was offered as a solution for this problem. Ultrasonic, or single plane welding technology, was not sufficiently advanced at that time to allow its immediate use. Therefore, standard resistance welding was selected. This type of welding requires a metal path from anode to cathode. Figure 7-7 shows the wafer designed for this purpose. The brazed-in metal balls provide the welding path. At a subsequent date a diode welding task was instituted. This task is still in progress as of this writing. The objective is to develop a process technique and capability of welding diodes directly to metalized ceramic wafers. Initial samples indicate that this objective will soon be realized.

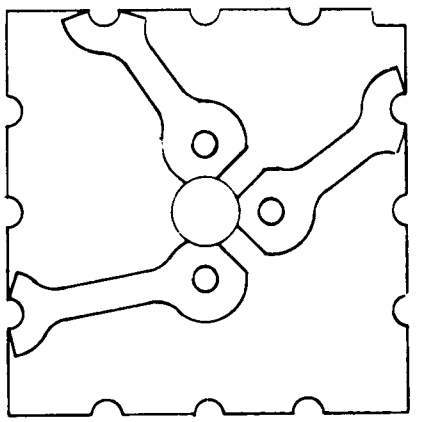


Figure 7-6a. Design Number 4, Mitronics

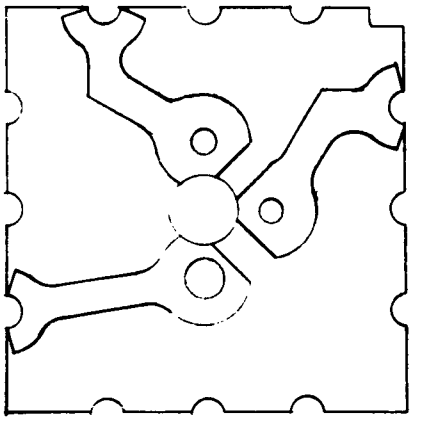


Figure 7-6b. Design Number 4 (Revised)

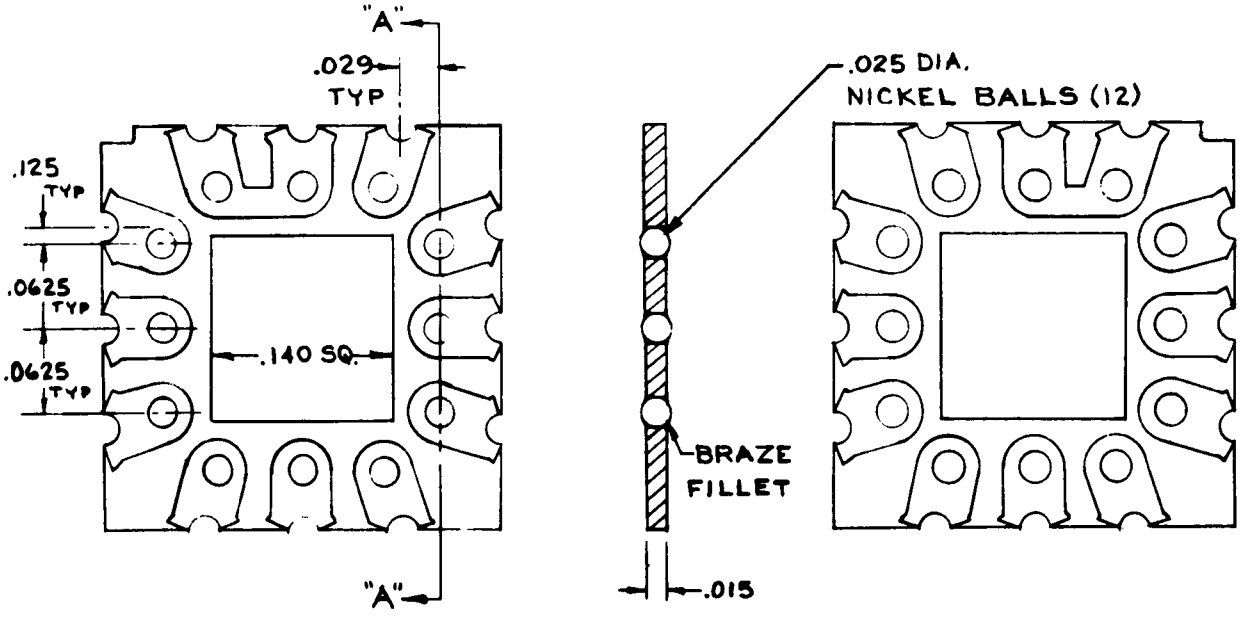


Figure 7-7. Diode Wafer, Mitronics

3.2 FABRICATION PROCEDURES AND EQUIPMENT

3.2.1 PROCESS DESCRIPTIONS

The following is a brief description of how ceramic wafers are produced at Mitronics. Some process details, considered proprietary by the vendor are not included.

Ceramic powder is mixed with organic binders to form a 96% alumina mixture. This mixture is cast into sheets of the desired thickness with allowances made for process shrinkage. The sheet, when cured, has a rubbery consistency and is then ready for stamping. The basic stamping die produces the standard outside dimensions of the wafer as shown in Figure 7-2. This die can be altered to provide a hole (or holes) of practically any shape within the wafer. The stampings are fired at 3000°F in a belt-fed oven. After firing, the wafers are inspected for flaws and for dimensional conformance. The moly-manganese metalization on the flat faces is applied by silk screen, and the notches are metalized by a proprietary process. The moly-manganese is then sintered to the alumina substrate in a hydrogen atmosphere belt fed furnace at 3000°F. The wafers are inspected for flaws in metalization and conformance to metal pattern dimensions. The metalized wafers are then given electrolytic deposits of nickel and gold. After inspecting the plating, the wafers are prepared for shipment by packaging.

3.2.2 PROCESS EVALUATION

The process described above is suitable for producing relatively small quantities at a premium price. In order to reduce costs, however, Coors Porcelain of Golden, Colorado, was given a contract to acquire facilities for larger quantity production. This contract was awarded under the PEM Program, Task 28-6.

3.3 TEST AND EVALUATION

The wafers produced in this task were inspected and tested for workmanship and functional use rather than strict conformance to specifications. It was of primary importance to produce usable wafers for prototype modules.

As stated before, the wafer shown in Figure 7-3 was selected as one of the final designs. A production quantity of the recessed hole wafer (Figure 7-5) was purchased from Ceramics for Industry for use with the Sylvania 0.250 inch package. The wafer shown in Figure 7-6a was not selected as one of the final design, but a separate purchase order was issued for a quantity to be supplied to the transistor manufacturers.

The prototypes of the wafer design shown in Figure 7-7 were tested by welding reject diodes to the wafer. The results obtained by use of a tweezer weld machine were outstanding. The joints were, in most cases, stronger than the wafer itself. This design was chosen as the second final design. Figure 7-8 is a photograph (magnification 4X) of wafers made to the above mentioned drawings.

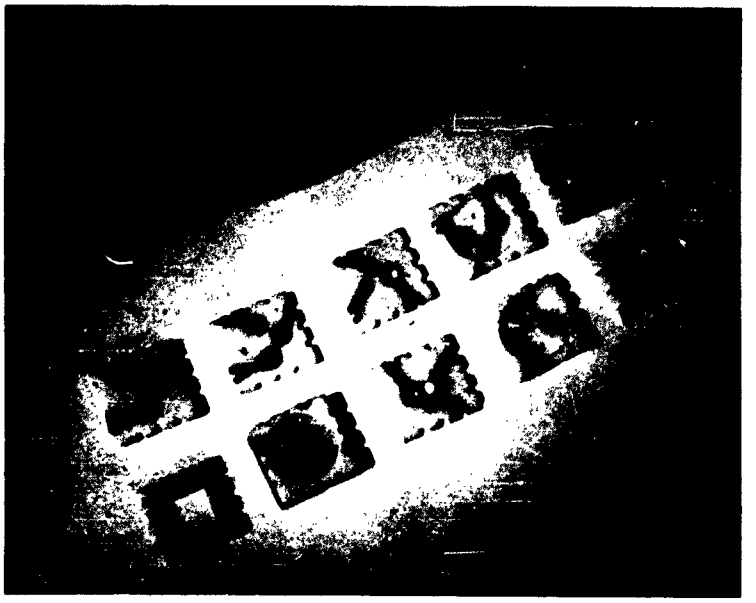


Figure 7-8. Ceramic Wafers of Task 18-7 (Magnification 4x) Made to Conform to the Drawings of Figures 7-3 through 7-7

3.4 UNIT SPECIFICATIONS

The specification governing this task was RCA Dwg. A-8948854 dated 15 August 1960, and as amended 30 September 1960. This document outlines the requirements for design and construction, materials, metalizing strength and dimensions, workmanship and quality assurance provisions. This specification was quite adequate for the task it performed but, in consideration of present requirements, it would fall short of specifying actual needs.

The module production personnel at RCA, Somerville, with the aid of experience and numerous vendor conferences, developed a specification for standard land and lead requirements. This document, RCA Dwg. 492984 entitled, "Standard Land and Lead Specification," is an accurate description of wafer requirements. As module production technology advances, this specification will be revised to reflect new requirements and to lessen or omit some of the present requirements.

3.5 DELIVERY

The contract awarded to Mitronics, Inc. originally called for delivery of twenty-five prototype samples each of five different designs by 30 November 1960. As previously stated, the wafer designs were released as the transistor packages became available.

Twenty-five samples of the wafer shown in Figure 7-3 were received in December of 1960. This design was chosen as a final type, and 1000 pieces were received in

January 1961, one month ahead of schedule. It also was originally intended that 1000 each of two selected final types be produced. Because of a need for prototype modules, two hundred additional units were delivered in April 1961, leaving a balance of 800 final wafers "on account."

Twenty-five each of wafers shown in Figures 7-4, 7-5 and 7-6 were received at RCA in February, March and June 1961, respectively.

Prototypes of the fifth and final wafer design (Figure 7-7) required from Mitronics were delivered in February 1962. Due to the complexity of this part and the considerably higher production costs, the requirement for 800 final units of this design was reduced to 200. The final shipment on this contract was received at RCA in September 1962.

The contract to Ceramics for Industry for recessed hole wafers called for 200 unmetalized samples as a feasibility study. Upon approval of these samples, 1000 metalized wafers were to be produced. The 200 samples for proving feasibility were due at RCA by January 31, 1961 but, due to technical difficulties, they were not received until March 11, 1961. Since the quality and workmanship was good, production of 1000 units was authorized. Five shipments of various quantities were received with the final quantity received in June 1961.

4. CONCLUSIONS AND RECOMMENDATIONS

This task produced the desired result, viz., the transistor manufacturers were supplied with ceramic wafers for mounting prototype transistors.

The quality of the wafers produced in this task was better than previously attained and has improved steadily with succeeding shipments. When this task was begun, precise requirements for microelement ceramic wafers were not yet formulated. With the advance of module production technology, the wafer requirements have become more clearly defined.

It is recommended that the wafer specifications be reviewed periodically to state new requirements and to omit or revise present requirements as the state-of-the-art advances.

The ceramic wafer is the building block of the micro-module and, since it will be used in huge quantities, every effort (e.g. PEM Task 28-6) should be employed to reduce unit cost.

SECTION VIII

FORMAL ENGINEERING REPORT
ON
MICROELEMENT VHF LOW POWER 2N1094 TRANSISTOR
TASK 18-8
MICRO-MODULE PROGRAM EXTENSION I

WESTERN ELECTRIC COMPANY
MARION AND VINE STREETS
LAURELDALE, PENNSYLVANIA

November 7, 1962

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. PURPOSE OF TASK 18-8

The primary objective of this program is to develop a very-high-frequency, diffused germanium transistor in a low height TO-46 package suitable for use in the micro-modules of the AN/PRC-51 Radio Set. The device should have characteristics similar to the 2N1094 transistor and must conform to the requirements of the RCA Specification 8978107.

2. ABSTRACT

Western Electric Co. fabricated 2N1094 wafers into the "pancake" TO-46 package using standard processing techniques with headers and cans from the Veritron West Company provided by RCA. One of the problems encountered was the bonding of the wafer to the platform. The glass insulator holding the lead on the header extended above the surface, causing difficult bonding. Standard eutectic bonding techniques were used. Leads were attached to the wafer using thermal compression bonding. Since initial requirements were insufficiently stringent for the primary intent of the program (AN/PRC-51 Radio Set), the specification was tightened. This action caused some of the units on test to be beyond specified limits. Since evaluation of the data would show any definite trends, tests were continued using the specimens available. Top priority of selection was for transistors necessary for the micro-modules. The remaining units were used for tests. Three transistor groups of different current gains (β) were required for the various circuits involved, for the sake of economy.

3. NARRATIVE AND DATA

3.1 DESIGN CONSIDERATIONS

No design objectives were encountered since this was a fabrication process.

3.2 FABRICATION PROCEDURES AND EQUIPMENT

3.2.1 DESCRIPTION OF PROCESS

Standard diffused-base manufacturing processes were used. Methods and techniques were modified where necessary to accommodate the TO-46 package.

3.2.2 EQUIPMENT

Standard test equipment was used.

3.2.3 EVALUATION OF PROCESS AND EQUIPMENT

Some automatic processing equipment is feasible such as automatic testing. However, no steps were taken under the present contract to automate any process.

3.3 TEST PERFORMANCE AND DATA

3.3.1 DESCRIPTION AND PURPOSE OF TESTS

The dc electrical (Group A) test as specified in Table 8-1 was performed on each transistor before subjecting any of them to subsequent tests.

3.3.2 ANALYSIS OF PERFORMANCE DATA

The results of the 2000 hour Storage Life (Group C) Test are presented in Figures 8-1, 8-2, and 8-3. Table 8-2 presents the "C" Test analysis.

The environmental (Group B) Test requirements and analysis are given in Table 8-3.

3.3.3 TEST PROCEDURES

Standard DC and AC testing procedures were used in accordance with the Standards Document, MIL-S-19500B.

3.3.4 CORRELATION OF DATA

Spot checks were performed between data taken by Western Electric and RCA for the same units. Differences seemed to be within the anticipated measurement error.

3.4 UNIT SPECIFICATIONS

(Including both package and wafers): The device is known as the "Pancake" transistor. The photograph of Figure 8-4 shows the 2N1094 both unmounted and mounted as a microelement. The specification governing these units was supplied through the combined efforts of Bell Telephone Labs and RCA. (RCA Dwg. #A-8978107, Amendment #1, dated 25 April 1962; Detail Requirements for a PNP diffused-base junction type VHF Germanium Transistor Microelement, similar to the 2N1094)

TABLE 8-1
ELECTRICAL MEASUREMENT ACCEPTANCE TESTS (GROUP A)

Test	Conditions	Sym.	Min.	Max.	Unit	Sample Size
Collector cut-off current	V_{CB} = -15v I_E = 0	I_{CBO}	-	3	ua	all
Collector cut-off current @ +85°C + 1°C - 3°C	V_{CB} = -15 I_E = 0	I_{CBO}	-	100	ua	all
Breakdown voltages	I_E = 0 I_C = -100uAdc	BV_{CBO}	-30	-	Vdc	all
	I_E = -100uAdc I_C = 0	BV_{EBO}	-1.5	-	Vdc	all
	I_B = 0 I_C = -100uAdc	BV_{CEO}	-15	-	Vdc	all
Output capacitance	I_E = 0 V_{CB} = -10Vdc	C_{ob}	-	2.5	uuf	all
Thermal resistance (4.1.2)	T_j = 100°C	O_{J-C}	-	75	°C/W	all
Type 1 Small signal short-circuit forward-transfer current ratio @25°C	f = 1kc V_{CE} = 5Vdc I_E = 1.0ma	h_{fe}	35	-	-	all
Small signal short-circuit forward-transfer current ratio @25°C	f = 1mc V_{CE} = 5Vdc I_E = 1.0ma	h_{fe}	30	-	-	all
Small signal short-circuit forward-transfer current ratio @-40°C	f = 1kc V_{CE} = 5Vdc I_E = 1.0ma	h_{fe}	15	-	-	all
Input impedance	I_E = 1mAdc V_{DB} = 6Vdc	h_{ib}	-	45	ohms	all
Reverse voltage transfer ratio	E = 1kc I_E = 1ma V_{CB} = -5Vdc	h_{rb}	-	.003	ohms	all

TABLE 8-1 (Continued)
ELECTRICAL MEASUREMENT ACCEPTANCE TESTS (GROUP A)

Test	Conditions	Sym.	Min.	Max.	Unit	Sample Size
Type 2						
Small signal short-circuit forward-transfer current ratio @25°C	f = 1kc V_{CE} = -5Vdc I_E = 1ma	h_{fe}	28	-	-	all
Small signal short-circuit forward transfer current ratio @-40°C	f = 1kc V_{CE} = -5Vdc I_E = 1ma	h_{fe}	11	-	-	all
Input impedance	I_E = 1mAdc V_{CB} = -5Vdc f = 50mc	h_{ib}	35 -30	70 -55	ohm uff	all
Reverse voltage transfer ratio	f = 50mc I_E = 1mAdc V_{CB} = 5Vdc	h_{rb}	-	0.03	-	all
Current gain @100mc	I_E = 1mAdc V_{CB} = 5Vdc	h_{fe}	9	-	db	all
Type 3						
Small signal short-circuit forward-current transfer ratio @25°C	f = 1kc V_{CE} = -5Vdc I_E = 1.0mAdc	h_{fe}	21	-	-	all
Small signal short-circuit forward current transfer ratio @-40°C	f = 1kc V_{CE} = -5Vdc I_E = 1.0mAdc	h_{fe}	10	-	-	all
Input Impedance	I_E = 1mAdc V_{CB} = -5Vdc f = 50mc	h_{ib}	28 16	31 21	ohm uff	all
Reverse voltage transfer ratio	f = 50mc I_E = 1mAdc V_{CB} = -5Vdc	h_{rb}	-	0.03	-	all

TABLE 8-1 (Continued)
ELECTRICAL MEASUREMENT ACCEPTANCE TESTS (GROUP A)

Test	Conditions	Sym.	Min.	Max.	Unit	Sample Size
Current gain @100mc	I_E = 1mAdc V_{CB} = -5Vdc	h_{fe}	9	-	db	all
Noise Figure	I_E = 1mAdc V_{CB} = -5Vdc R_g = 600Ω	NF	-	12	db	all

3.5 PRODUCT EVALUATION

The h_{fe} of the transistors tested shows a tendency to increase with aging and I_{CBO} values tend to decrease. Reliability should equal that of the standard transistor package. The transistors functioned satisfactorily in the circuits of the modules for the AN/PRC-51, but improvement is desirable.

3.6 DELIVERY

Date	Quantity	Date	Quantity
12/16/60	35	11/28/61	92
12/21/60	50	12/26/61	201
5/15/61	45	12/28/61	35
7/12/61	82	12/18/61	87
9/26/61	50	12/14/61	92
9/29/61	35	12/12/61	143
11/17/61	52	12/5/61	101
		Total Delivered	1,100 Units

TABLE 8-2
FAILURE RATE AND ANALYSIS FROM STORAGE LIFE (GROUP C) TESTS

FAILURE RATE

ENVIRONMENT	DEGRADATION		INOPERABLE	
	MTBF	FRACTION DEF.	MTBF	FRACTION DEF.
100°C Storage Life 1000 hrs	110,000 hrs (60% confidence)	.0091 per 1000 hrs	243,000 hrs (60% confidence)	.0041 per 1000 hrs

TYPE TESTED
2N1094
SPECIFICATION
A-8978107, Amend. 1
DATE ISSUED (Spec)
25 April 1962

FAILURE ANALYSIS

SAMPLE SIZE	TOTAL HOURS	FAILURES	250 HOUR FAILURES	500 HOUR FAILURES	1000 HOUR FAILURES
223	223,000	1 h_{FE} degradation			1 (h_{FE})

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS TA = 25°C	INITIAL LIMITS		END OF LIFE LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	V_{CB} - 15V I_E = 0		3.0 μA		6.0 μA		6.0 μA
h_{FE}	V_{CE} - 5V I_E = 1ma						
Type 1	f = 1kc	35		30		30	
Type 2		28		25		25	
Type 3		21		18		18	

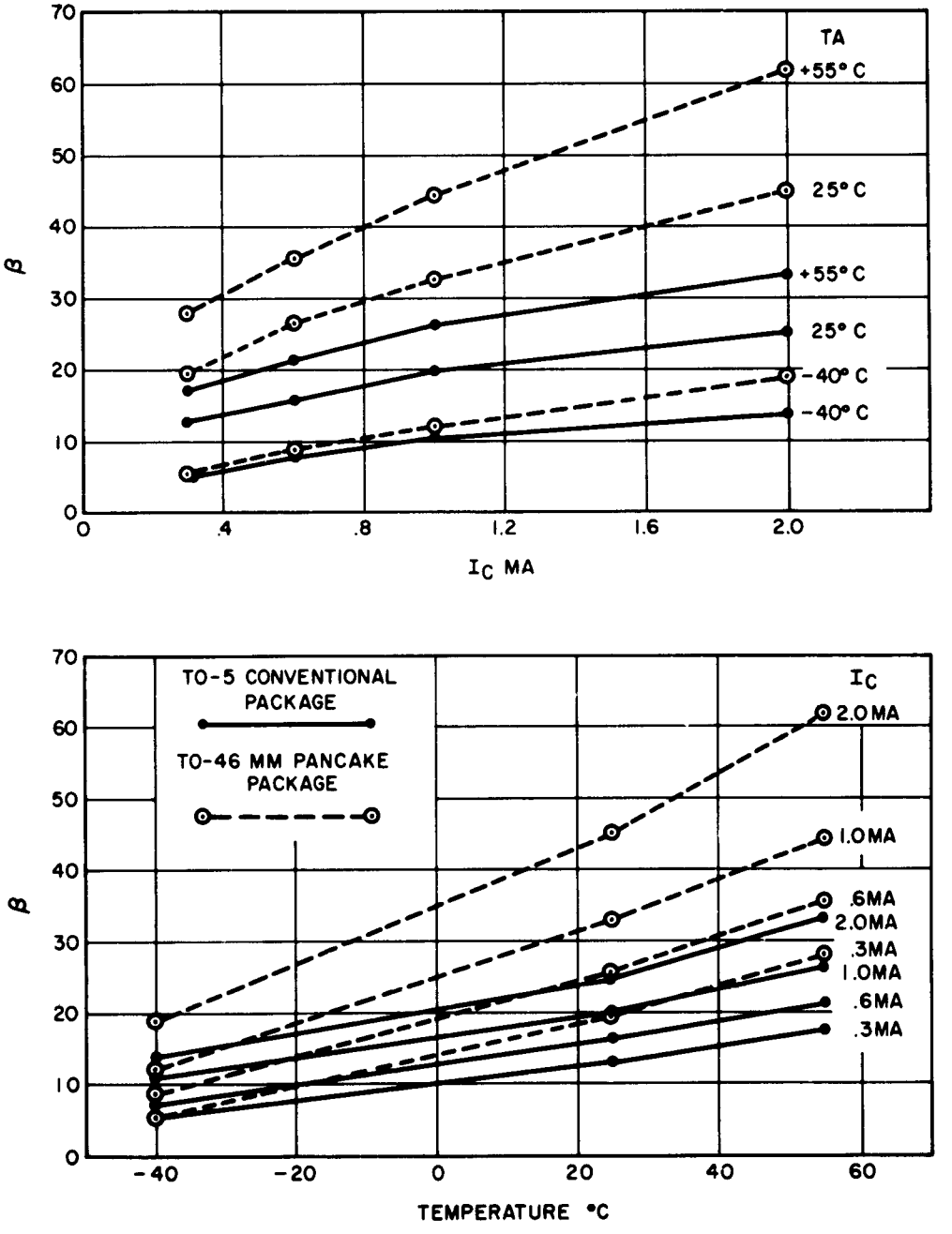


Figure 8-1. Current Gain (β) vs. Collector Current and Temperature for Western Electric 2N1094 Transistor

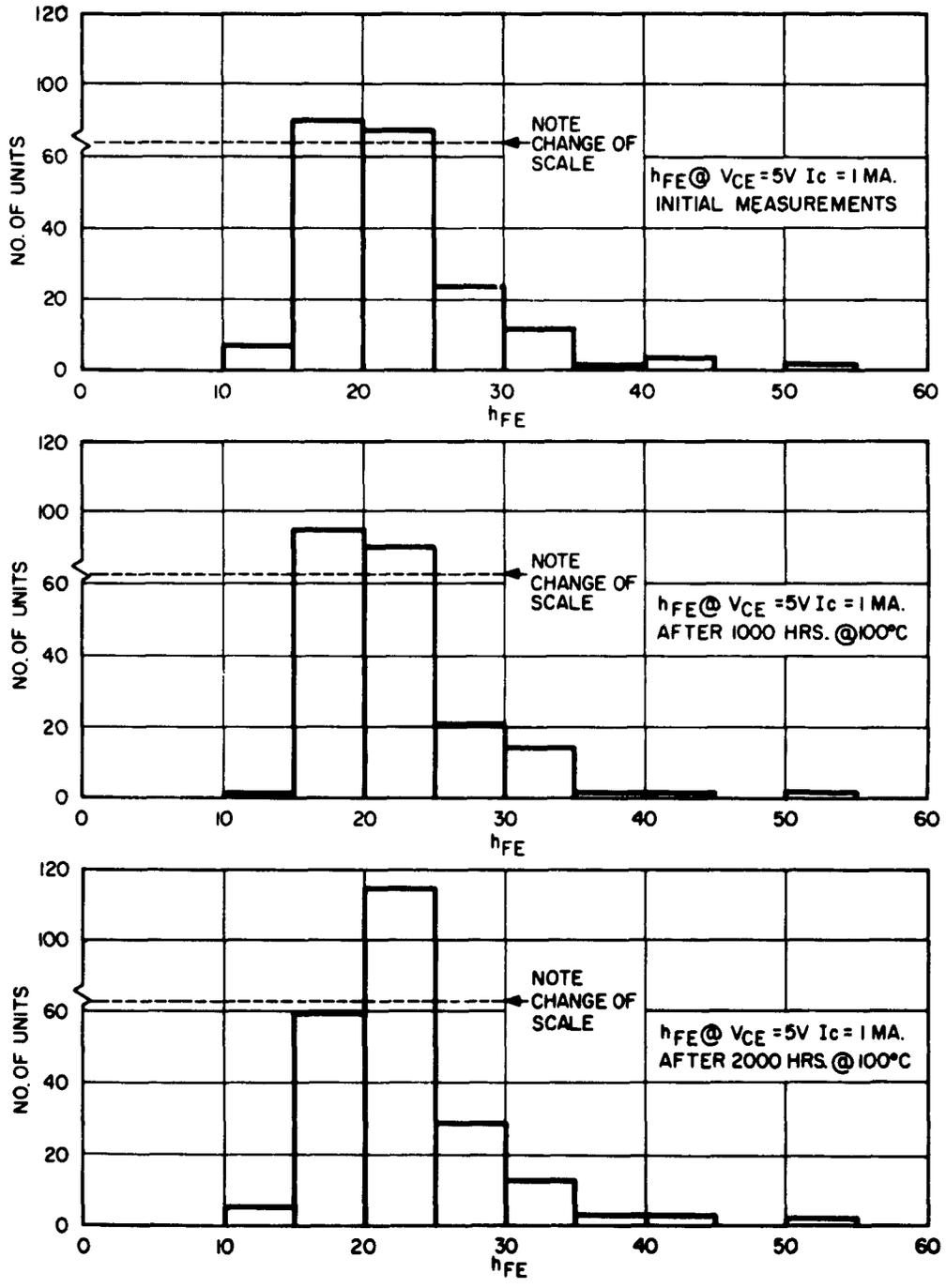


Figure 8-2. Graphs of Units vs. h_{FE} after 0, 1000, and 2000 Hours of Storage Life Test for 223 Western Electric 2N1094 Transistor

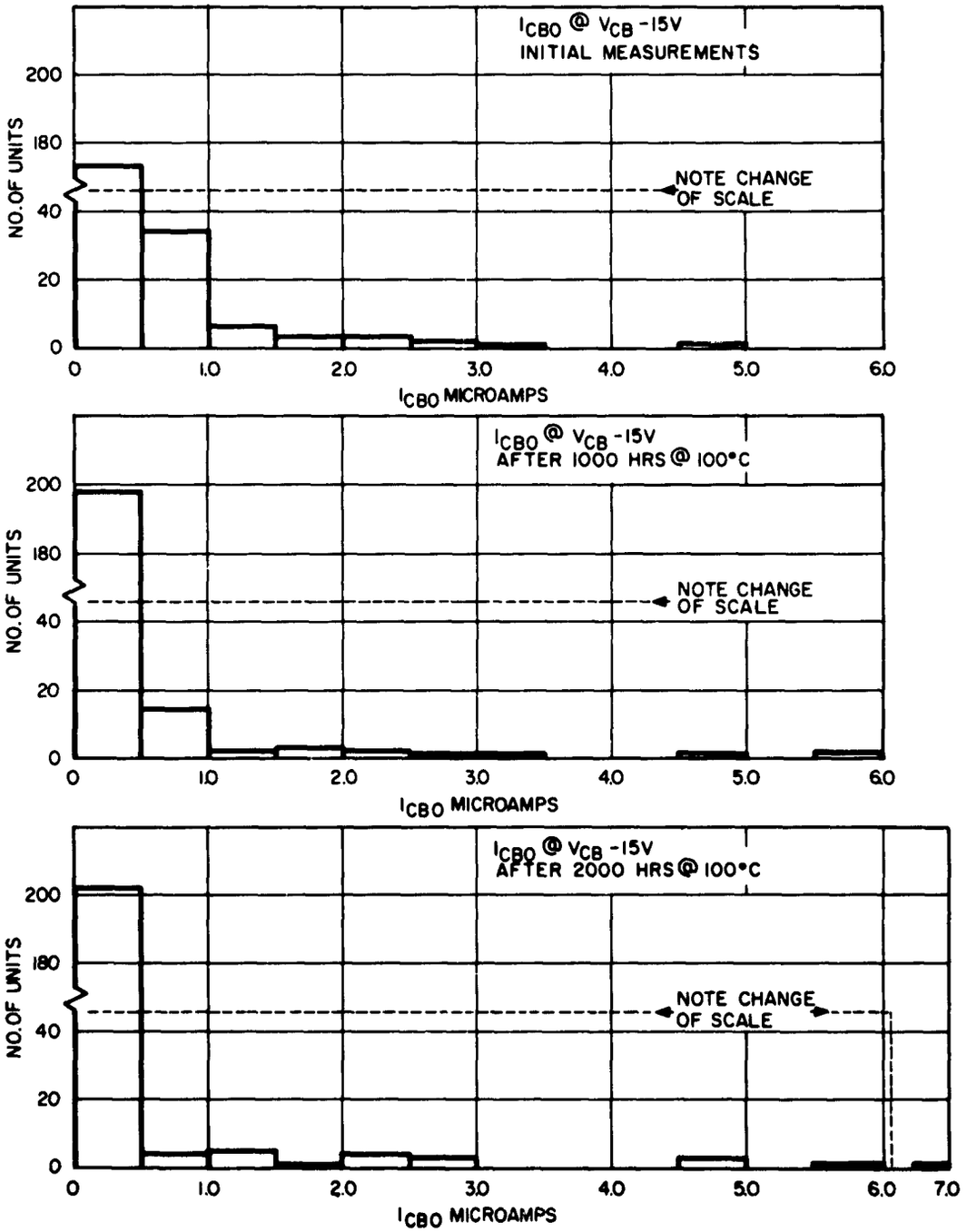


Figure 8-3. Graphs of Units vs. I_{CBO} after 0, 1000, and 2000 Hours of Storage Life Test for 223 Western Electric 2N1094 Transistor

TABLE 8-3
ANALYSIS OF ENVIRONMENTAL (GROUP B) TESTS

SUB-GROUP	TEST AND SPECIFICATION
I	a. Thermal Shock - 107 of MIL-STD-202B, Cond. A b. Moisture Resistance - 106A of MIL-STD-202B, 10 cycles
II	a. Centrifuge-4.6.2.9 of MIL-T-19500A (20,000 g) b. Vibration-204 of MIL-STD-202B, Cond. C (non-operating)
III	a. Altitude-105A of MIL-STD-202B, 104" Mercury

TYPE TESTED 2N1094
SPECIFICATION A-8978107, Amend. 1
DATE ISSUED (Spec) 25 April 1962

SUB-GROUP	ENVIRONMENTAL CONDITIONS
I	a. 5 cycles @ −55°C 30 min., 25°C 10 min., 85°C 30 min., 25°C 10 min. b. Ten 24 hour cycles variable temperature (25 to 65°C) c. Relative humidity (90 to 95%)
II	a. 4 Orientations, one minute duration at 20,000 g. b. 2 hours in each of 3 orientations, .06" max., 10-55-10 cps in 1 min. and 55 to 2000 cps in 35 ± 5 minutes in 3 orientations
III	a. Altitude Chamber was maintained at .04" of mercury for 30 minutes

FAILURE ANALYSIS

SAMPLE SIZE	SUB-GROUP	FAILURES	CLASSIFICATION OF FAILURES
15	I	1	Ib - h_{FE} dropped below minimum requirement
6	II	1 (intermittent)	IIa - I_{CBO} affected by tapping the case
6	III	0	

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS TA = 25°C	INITIAL LIMITS		POST TEST LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	V_{CB} = 15V I_E = 0		3.0 μA		4.5 μA		4.5 μA
h_{FE}	V_{CE} = 5V I_E = 1.0 ma f = 1 kc						
Type 1		35		32		32	
Type 2		28		25		25	
Type 3		21		19		19	

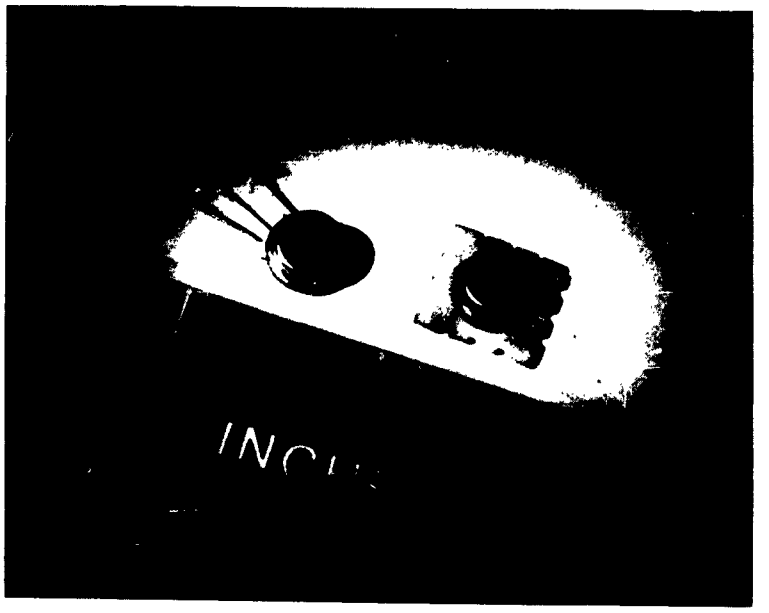


Figure 8-4. Views of the 2N1094 Microelement Transistor (Magnified 5x)

4. CONCLUSIONS AND RECOMMENDATIONS

4.1 CONCLUSIONS

A "Pancake" type transistor using the TO-4C package was successfully fabricated which met the requirements set forth by RCA and the Signal Corps. No state-of-the-art conclusions can be made here because of the small number of devices involved.

4.2 RECOMMENDATIONS

Some r-f applications require isolation of the collector from the transistor can. This will minimize radiation and feedback in r-f circuits. A new package design resulting in an isolated collector would be desirable.

SECTION IX

FORMAL ENGINEERING REPORT
ON
MICROELEMENT 2N404 TRANSISTOR,
TYPES A-1 and A-2
TASK 18-9
MICRO-MODULE PROGRAM EXTENSION I

PO GX1-946254-8142-24-D38

SYLVANIA ELECTRIC PRODUCTS
WOBURN, MASSACHUSETTS

November 15, 1962

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. PURPOSE OF TASK 18-9

The purpose of the contract was to fabricate and deliver PNP germanium alloy transistors to the RCA specification #8972092. The transistors are of a variety electrically similar to the 2N404, but of a packaging type suitable for use as micro-elements in micro-modules with electrical, mechanical, and environmental conformance to the applicable specifications and purchase order.

2. ABSTRACT

The attached summary and accompanying process specifications describe the manner in which the PNP germanium alloy micro-module transistor was fabricated for RCA. All available pertinent information of a non-proprietary nature has been included in this report.

Standard PNP transistor line processes and manufacturing techniques were used with the exceptions of the enclosure, and the tab structure which was necessarily altered to minimize the size of the device. The enclosure comprises a resistance welded Kovar header cap and leads with terminal seals of hard glass. Care must be exercised in testing and handling the transistors as the hard glass seals are easily cracked. Test measurements indicate a slight increase in I_{CBO} after the second 1000 hours, as exhibited in the enclosed graphs.

3. NARRATIVE AND DATA

3.1 DESIGN CONSIDERATIONS

3.1.1 PACKAGE AND CLOSURE

The package was chosen to be of the resistance weld type due to the successful hermetic seal and cleanliness of this variety. It was designed by Sylvania as a resistance-welded hermetic enclosure consisting of a kovar stamping with kovar terminals sealed in with #7052 (hard) glass in a stress-free oxide seal.

This part is listed in Section 3.2.1.1 as item 8. Lead wires were .014" in diameter in order to provide enough current-carrying capacity and sufficient stiffness to allow direct insertion into printed circuit boards or (possibly) wafers. The entire package is tin-plated for corrosion resistance.

3.1.2 ALLOYED ASSEMBLY

The alloyed assembly was identical to the type used in the manufacturing of TO-5 packaged transistors, except for the tab structure. The tab was designed to fit the header pedestal evenly. It was made of nickel .006" in thickness and was plated with tin-lead for germanium die adherence. The inside diameter was chosen the

same as that of the standard TO-5 line, viz., .030". The total geometry remained the same as for the 2N404 transistor line; however, an effective decrease in dimensions was made wherever possible.

3.2 FABRICATION PROCEDURES AND EQUIPMENT

3.2.1 DESCRIPTION OF PROCESS

3.2.1.1 COMPONENT PARTS

1. Germanium Die
2. Collector Dot
3. Emitter Dot
4. Tab
5. Connecting Wire
6. Solder
7. Flux
8. Header
9. Encapsulant
10. Cap

3.2.1.2 PREPARATION, INSPECTION, AND ASSEMBLY

Component parts were cleaned, prepared, inspected, and assembled using standard PNP production line techniques with Quality Control and Process Control maintaining production variables both of the processes and of the process equipment. The Process Flow Chart is presented in Figure 9-1. Figure 9-2 shows the Transistor Junction Assembly. Figures 9-3 and 9-4, respectively, are line drawings of the Cap of the enclosure and the Header (Stem) Assembly.

3.2.2 FABRICATION EQUIPMENT

The assembly and fabrication equipment used for the Microelement 2N404 was identical to that used for the conventional transistor.

3.2.3 EVALUATION OF PROCESS AND EQUIPMENT

Standard PNP transistor line techniques were used. State-of-the-art equipment was modified where necessary to accommodate the package.

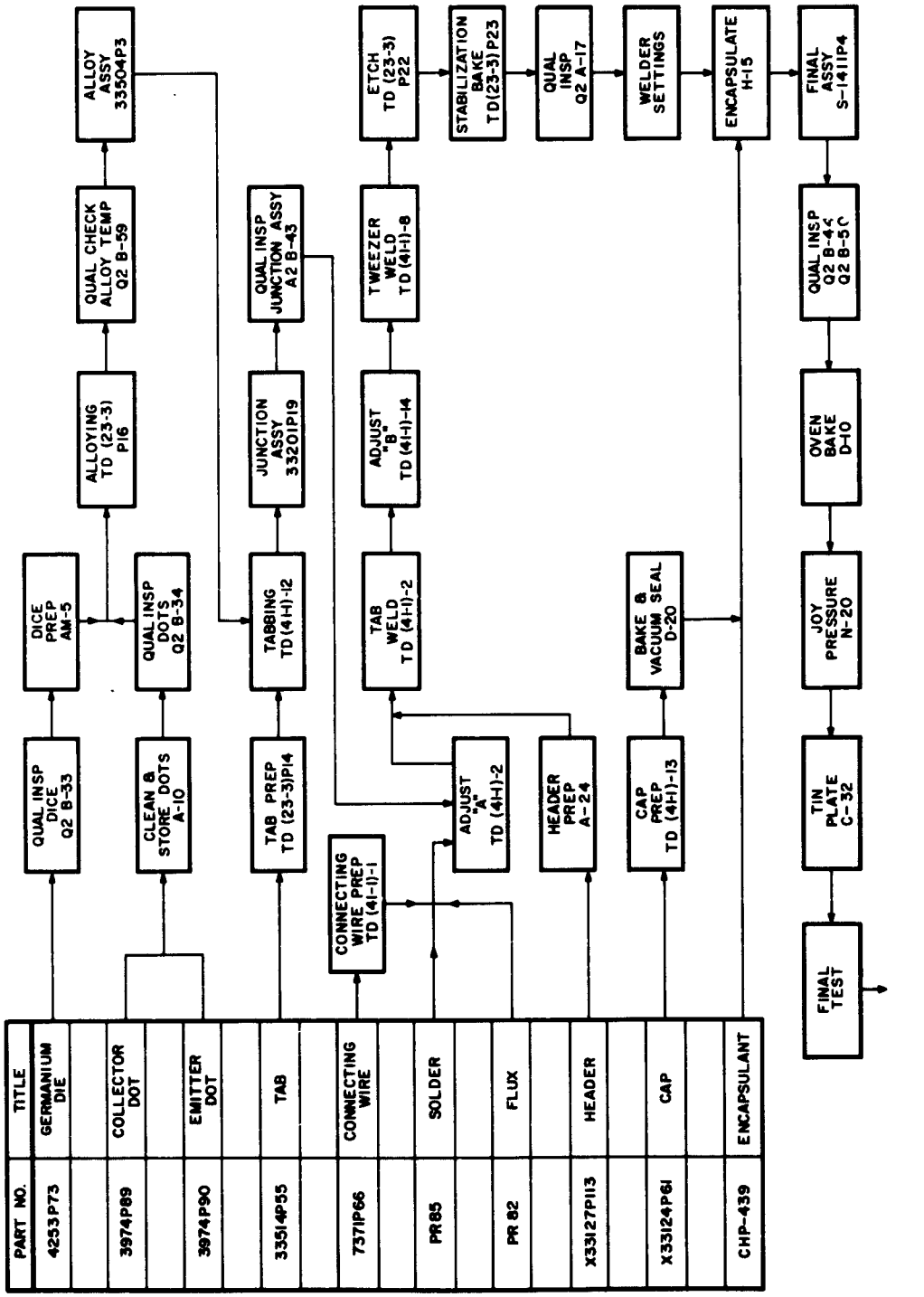
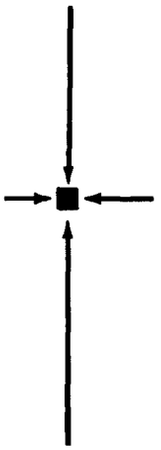


Figure 9-1. Process Flow Chart



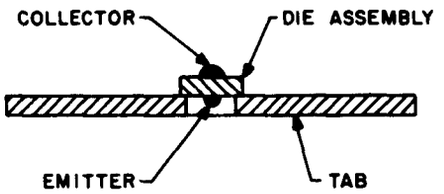
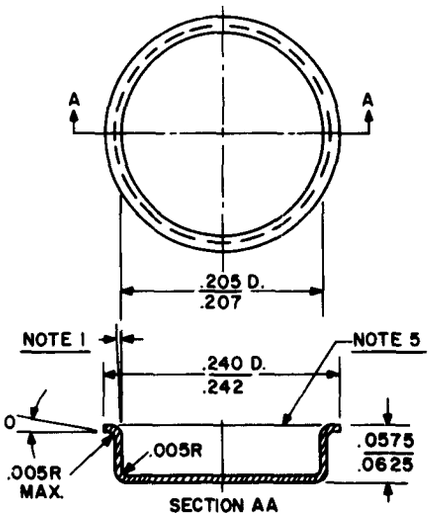


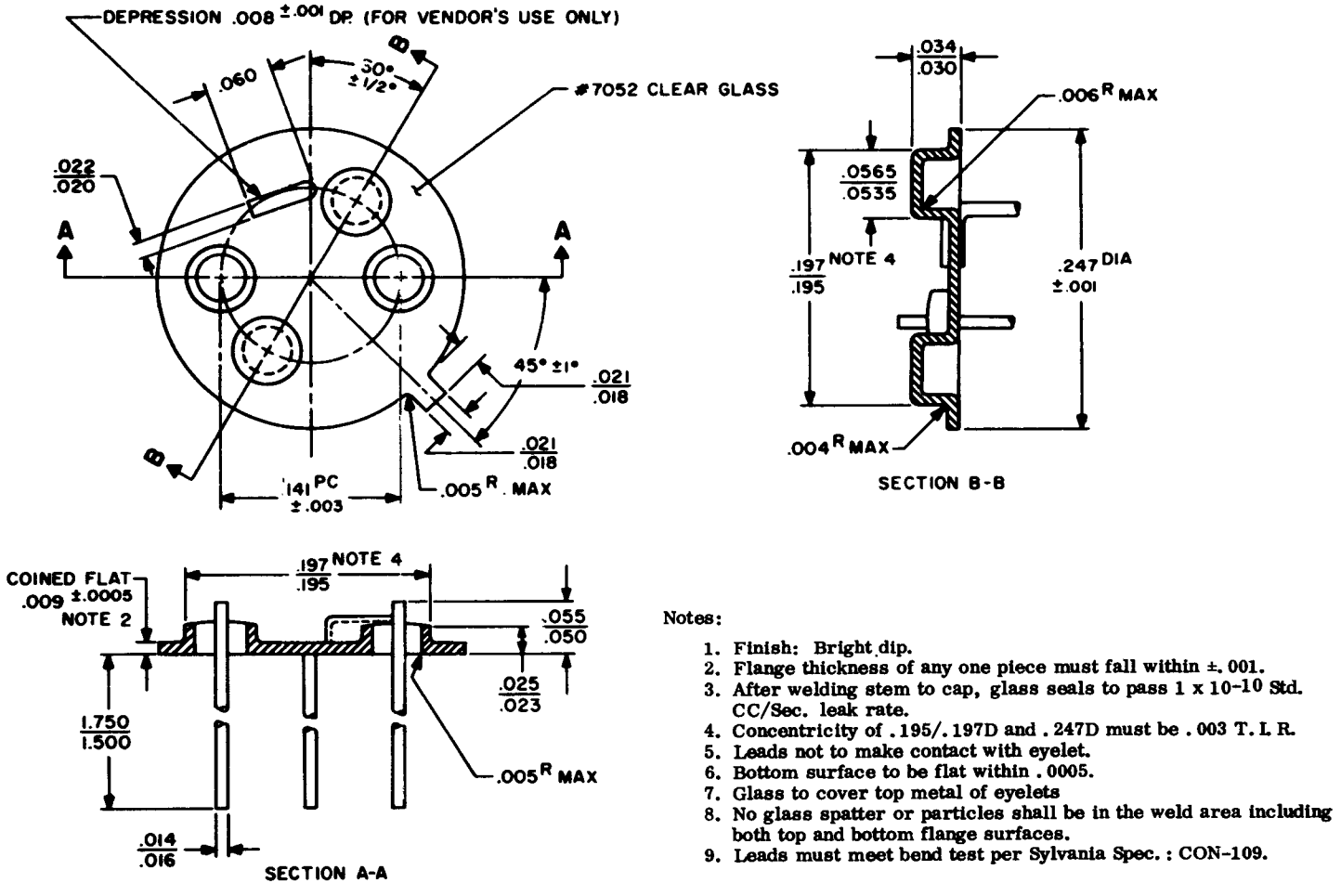
Figure 9-2. Transistor Junction Assembly



Notes:

1. 1° max. taper inside of shell.
2. Body to flange eccentricity . 002 max. T. I. R.
3. Thickness of flange must not vary more than ±. 0005.
4. Part to be cleaned by firing in a hydrogen atmosphere furnace at 900°C for 20 min keep entirely surrounded by gas to 200°C pack in air tight containers while still as hot as practicable.
5. Flange to be flat within . 001 with face free of burrs.

Figure 9-3. Cap



Notes:

1. Finish: Bright dip.
2. Flange thickness of any one piece must fall within ±. 001.
3. After welding stem to cap, glass seals to pass 1 x 10^{-10} Std. CC/Sec. leak rate.
4. Concentricity of .195/.197D and .247D must be .003 T. I. R.
5. Leads not to make contact with eyelet.
6. Bottom surface to be flat within .0005.
7. Glass to cover top metal of eyelets
8. No glass spatter or particles shall be in the weld area including both top and bottom flange surfaces.
9. Leads must meet bend test per Sylvania Spec. : CON-109.

Figure 9-4. 2N404 Transistors Header Assembly (Stem)

3.3 TEST PERFORMANCE AND DATA

3.3.1 DESCRIPTION AND PURPOSE OF TESTS

In-process and Quality Control tests were performed to maintain control of production variables, and to evaluate device reliability and compatibility with the specifications.

3.3.2 ANALYSIS OF PERFORMANCE DATA

3.3.2.1 RESULTS OF THE ELECTRICAL PERFORMANCE (GROUP A) TESTS ARE EXHIBITED IN TABLE 9-1

3.3.2.2 SUMMARIES AND ANALYSES OF STORAGE LIFE (GROUP C) AND OF ENVIRONMENTAL (GROUP B) TESTS ARE GIVEN IN TABLES 9-2 AND 9-3, RESPECTIVELY

3.3.2.3 DISTRIBUTION GRAPHS OF I_{CBO}, h_{fe}, and BV_{CEV} VALUES AFTER 1000 HOURS AND 2000 HOURS OF STORAGE LIFE (GROUP C) TESTS ARE PRESENTED IN FIGURES 9-5, 9-6, AND 9-7.

3.4 UNIT SPECIFICATIONS

3.4.1 TEST SPECIFICATIONS

	MIN.	MAX.
I_{cbo} @ V_{cb} = -16V	-	10 ua
I_{ebo} @ V_{eb} = -.5V	-	12 ua
BV_{cex} @ V_{eb} = -.5V Ic = .01 ma	16V	-
f_{ab} @ V_{eb} = -6V Ic = 1 ma	4 mc	20 mc
h_{fe} @ V_{ce} = -6V, Ic = 1 ma f = 1 KC	25	180

The transistors were tested to meet the above requirements within a 1.0% combined acceptance quality level.

TABLE 9-1
ELECTRICAL REQUIREMENTS OF ACCEPTANCE (GROUP A) TESTS

Test	Conditions	Sym.	Min.	Max.	Unit
Group A Visual and mechanical	3.7 of RCA Dwg. A-6972091	-	-	-	-
Emitter cut-off current	V_{EB} = -0.5V I_C = 0	I_{EBO}	-	-12	ua
Collector voltage	I_C = 10 ua V_{EB} = -0.5V	BV_{CEV}	-16	-	volts
Short circuit small-signal forward current transfer ratio					
Type A-1	f = 1 kc V_{CE} = -6V I_E = 1 ma	h_{fe}	25	90	-
Type A-2	f = 1 kc V_{CE} = -6V I_E = 1 ma	h_{fe}	85	180	-
Alpha cut-off frequency	V_{CB} = -6V I_E = 1 ma	f_{ab}	4	20	mc
Output capacitance	V_{CB} = -6V I_E = 0	C_{ob}	-	15	mf
Converter gain	V_{CE} = -6V	CG	25	-	db

TABLE 9-2
ANALYSIS OF STORAGE LIFE (GROUP C) TESTS

FAILURE RATE				
ENVIRONMENT	DEGRADATION		INOPERABLE	
	MTBF	FRACTION DEF.	MTBF	FRACTION DEF.
100°C Storage Life 1000 hrs	64,300 at 60% confidence	.0156 per 1000 hrs	100,000 at 60% confidence	.010 per 1000 hrs

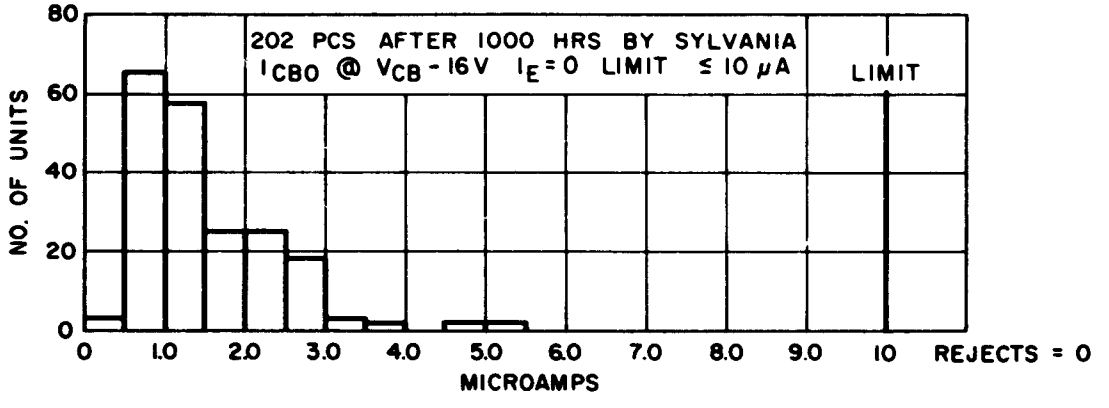
TYPE TESTED
2N404
SPECIFICATION
A-8972092, Rev. B Amend. 2
DATE ISSUED (Spec)
11 May 1961

FAILURE ANALYSIS

SAMPLE SIZE	TOTAL HOURS	FAILURES	250 HOUR FAILURES	500 HOUR FAILURES	1000 HOUR FAILURES
202	202,000	2 I_{CBO} (degradational) # 98,19 μA #171,18 μA	–NWT intermittent		2 I_{CBO}

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS	INITIAL LIMITS		END OF LIFE LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	V_{CB} = –16V, I_E = 0				15 μA		15 μA
I_{EBO}	V_{EB} = –.5V, I_C = 0		12 μA		18 μA		18 μA
BV_{CEV}	I_C = –10 μA, V_{EB} = –.5V	–16V					
h_{FE}	V_{CE} = –6V						
Type 1	I_E = 1 ma	25	90	20		20	
Type 2	f = 1 kc	85	180	70		70	
BV_{CEV}	I_C = –10 μA, V_{EB} = –.5V	–16V					



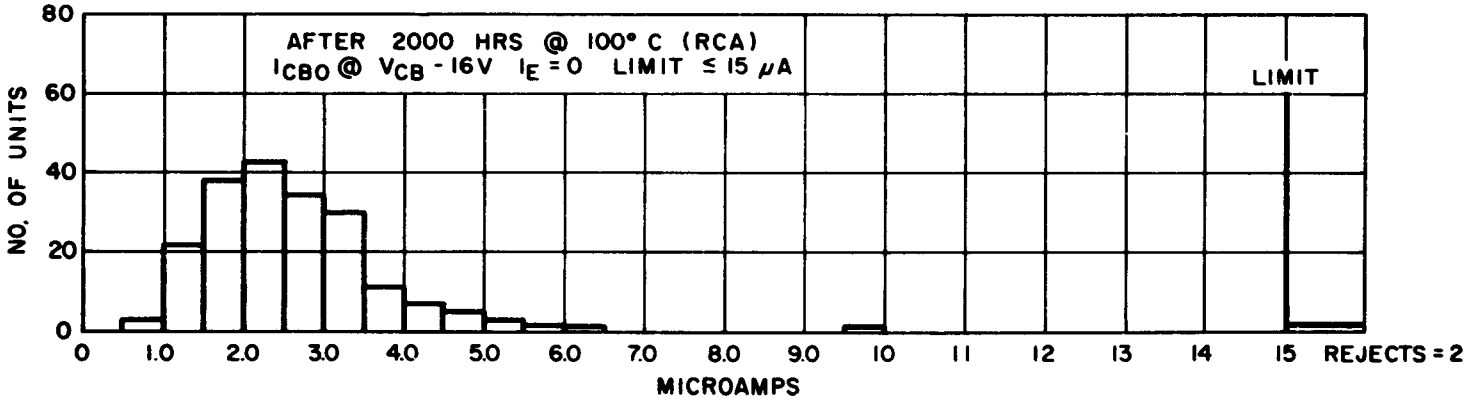


Figure 9-5. Units vs. I_{CBO} after Storage Life Tests on Sylvania 2N404 Microelement Transistors

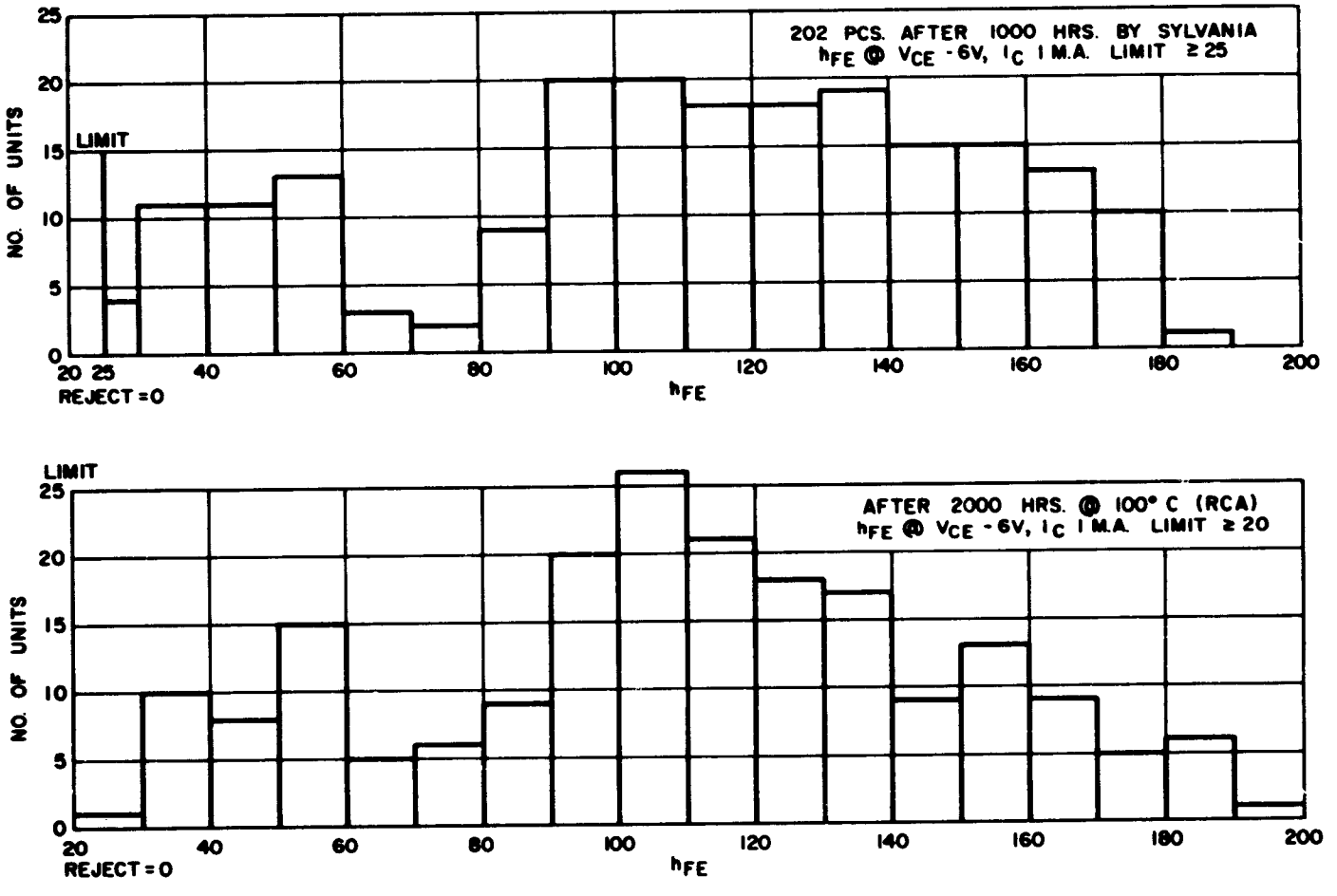


Figure 9-6. Units vs. h_{FE} after Storage Life Tests on Sylvania 2N404 Microelement Transistors (Magnification 5x) Compared

TABLE 9-3
ANALYSIS OF ENVIRONMENTAL (GROUP B) TESTS

SUB-GROUP	TEST AND SPECIFICATION
I	a. Thermal Shock - 107 of MIL-STD-202B, Cond. A. b. Moisture Resistance - 106A of MIL-STD-202B, 10 cycles
II	a. Centrifuge - 4.6.29 of MIL-T-19500A (20,000 g) b. Vibration - 204 of MIL-STD-202B, Cond. C, (non-operating)
III	a. Altitude - 105A of MIL-STD-202B, .04" mercury

TYPE TESTED
2N404
SPECIFICATION
A-8972092, Rev. B Amend. 2
DATE ISSUED (Spec.)
11 May 1961

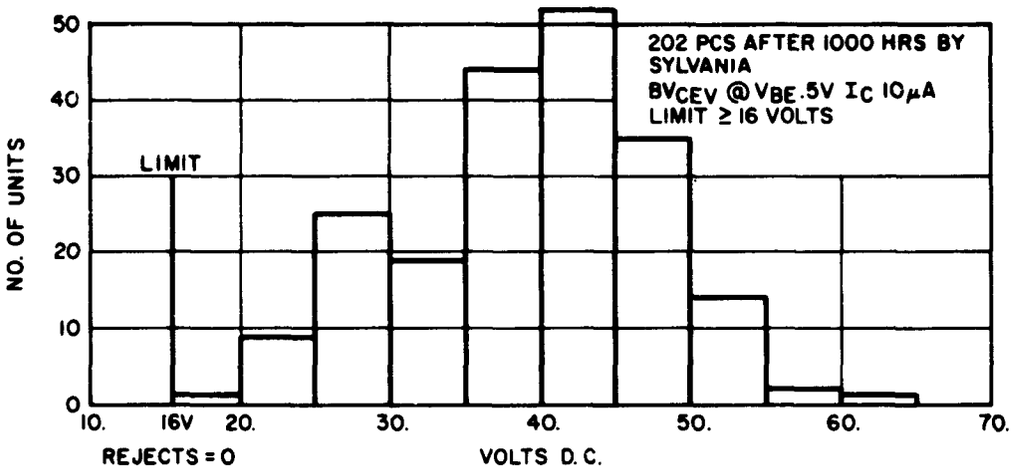
SUB-GROUP	ENVIRONMENTAL CONDITIONS
I	a. 5 cycles at -55°C, 30 min., 25°C, 10 min., 85°C, 30 min., 25°C, 10 min. b. Ten 24 hour cycles variable temperature (25° to 65°C) relative humidity (90 - 95%).
II	a. 4 orientations, one minute duration at 20,000 g. b. 2 hours in each of 3 orientations, .06" max. 10-55-10 cps in 1 min. and 55 to 2000 cps in 35 ± 15 minutes in 3 orientations
III	a. Altitude chamber was maintained at .04" of mercury for 30 minutes.

FAILURE ANALYSIS

SAMPLE SIZE	SUB-GROUP	FAILURES	CLASSIFICATION OF FAILURES
15	I	a. 0 b. 0	
6	II	a. Fixture not available b. 0	
6	III	a. 0	

FAILURE DEFINITIONS

PARAMETER	TEST CONDITIONS	INITIAL LIMITS		POST TEST LIMITS		INOPERABLE LIMITS	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
I_{CBO}	V_{CB} = -16V, I_E = 0				15 μA		15 μA
I_{EBO}	V_{EB} = -.5V, I_C = 0		12 μA		12 μA		12 μA



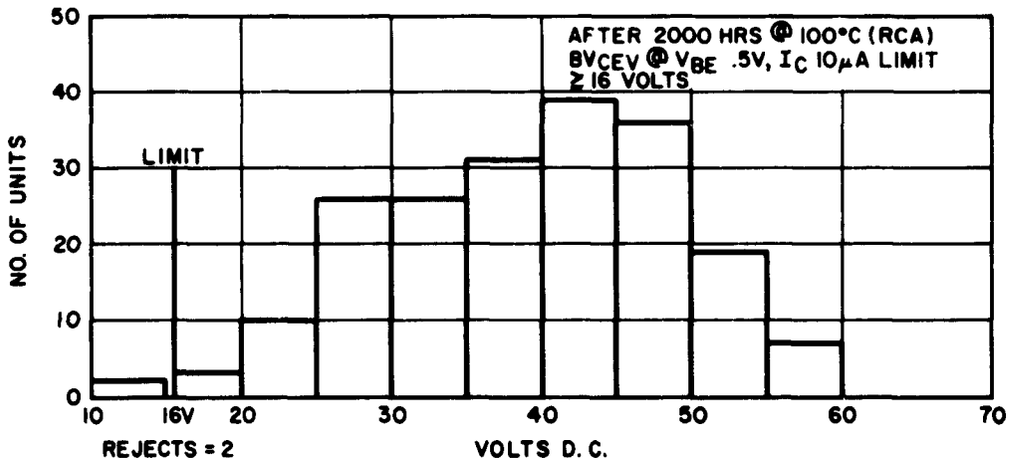


Figure 9-7. Units vs. BV_{CEV} after Storage Life Tests

3.4.2 RCA SPECIFICATION A-8972092 REVISION B, AMENDMENT 2, DATED 11 MAY 1961

MAXIMUM RATINGS

V_{cb}	I_c	V_{eb}	I_c	TA	Pc	Tstg.	T_j
-16 VCD	-15 MA	-.5 VDC	15 MA	85°C	80 Min.	-55 to 100°C	100°C

3.5 PRODUCT EVALUATION

This device, shown in the photograph of Figure 9-8, has characteristics similar to the standard 2N404 (TO-5 package). The prime objective of this task was to shrink the dimensions to obtain a compatible device for the Micro-Module Program. A kovar package and leads with glass seals was chosen and resistance-welding was used for reliability and conformance to the environmental requirements of the specifications.

3.6 DELIVERY

Quantity	Date Due	Quantity	Date Received	
100	8/1/61	80	8/15	
		20	8/28	
200	11/1/61	200	9/18/61	Cracked glass seals due to improper handling returned to SYL 12/12/61
		200	3/ /62	
		40	5/ /62	
		17	5/17/62	
		16		

4. CONCLUSIONS AND RECOMMENDATIONS

4.1 CONCLUSIONS

With state-of-the-art processes and techniques the 2N404 microelement transistor reliability should equal that of any other transistor in production.

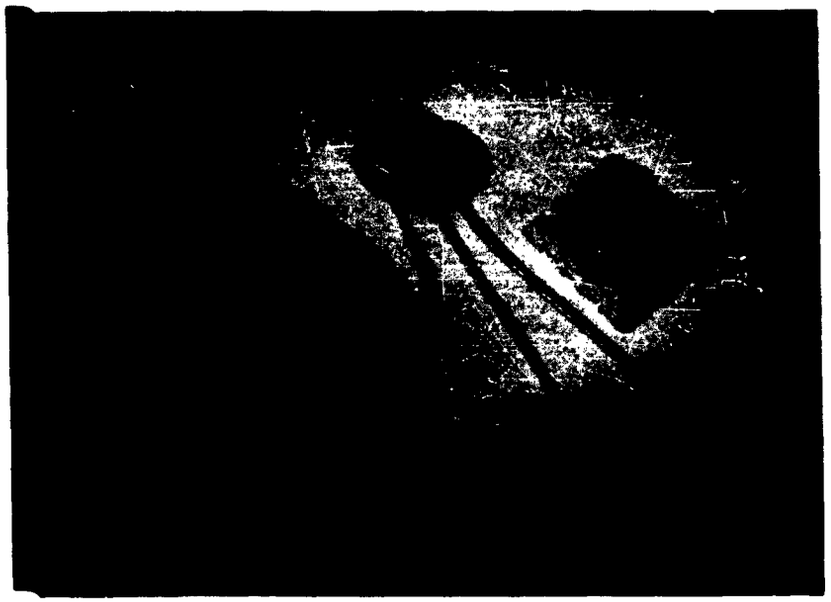


Figure 9-8. Microelement 2N404 Transistor (Magnification 5x) Compared in Size with a Lincoln Penny

Non conforming units were found and close examination led to the discovery of cracked glass seals. Sylvania contended that improper handling at RCA caused the problem; however, examination of samples at Sylvania also showed cracked glass. Test jigs and handling procedures were modified to prevent undue stress on the hard glass seals caused by bending of the leads. Care in handling and closer inspection of the header assembly resolved this problem. Subsequent tests, examination, and data displayed conformance with the specified requirements.

4.2 RECOMMENDATIONS

Upon successful completion of this task, Sylvania stopped production of alloy junction transistors. If there is a large volume requirement for the microelement 2N404 transistor, Sylvania will resume production. In order to satisfy small quantity needs, it would be advisable to establish a second source for the microelement 2N404 transistor.